O B A L

MNK L

- Wide Input Voltage Range: 2.7V-12V
- Wide Output Voltage Range: 4.5V-12.6V
- Fully Integrated 17
  14
- Up to 93% Efficiency at Vin=3.3V, Vout=9V, and Iout=2A
- Programmable and Up to 9.5A Peak Switch Current Limit
- Typical Shut-down Current: 1uA
- Quiescent Current: 150uA
- Adjustable Switching Frequency: 200KHz to 2.2MHz
- PFM Operation Mode at Light Load
- Internal Soft Start and External Compensation
- Cycle-by-Cycle Overcurrent Protection
- Output Overvoltage Protection
- Thermal Shutdown Protection: 160°C
- QFN-11 2mm x 2.5mm Package

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- Bluetooth Speaker
- Portable POS Terminal
- Quick Charge Power Bank
- E-Cigarette
- Outdoor Flashlight

L KBI MBHG

The SCT1270 is a high efficiency synchronous boost converter with fully integrated a 17 high-side MOSFET and a 14 low-side MOSFET, featuring 2.7V to 12V input voltage range to support single cell or two cell Lithium ion/polymer batteries and up to 9.5A peak switch current. The switch current limit can be adjustable with an external resistor. The SCT1270 has 7A continuous switch current capability and provides output voltage up to 12.6V.

The SCT1270 adopts constant off-time peak current control to provide fast transient response. An external compensation network allows flexibility setting loop dynamics to achieve optimal transient performance at different load conditions.

The SCT1270 works in the PWM at moderate and heavy load condition. The SCT1270 offers PFM mode at light load condition. The switching frequency is adjustable from 200KHz to 2.2MHz.

The SCT1270 features output overvoltage protection and thermal shutdown protection when the device over loads.

The device is available in a QFN-11 2mm x 2.5mm package.

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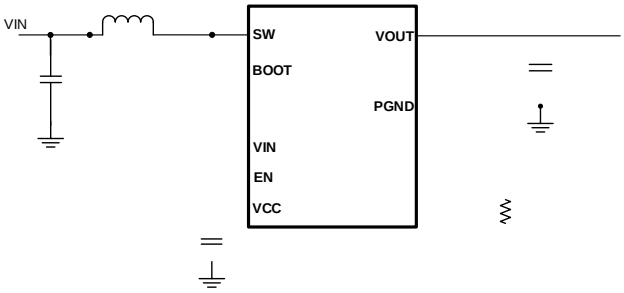

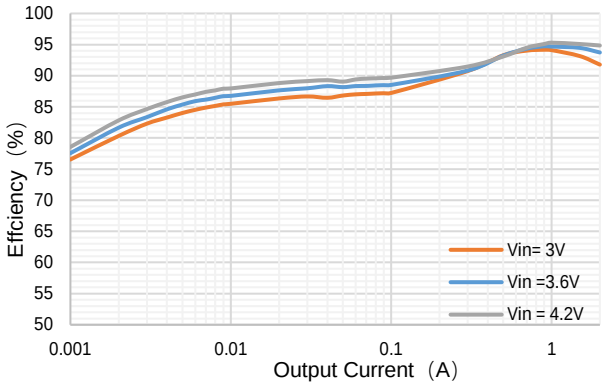

Efficiency vs Load Current, Vout=9V

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

Revision 1.1: Update T_J to 150 ºC

Revision 1.2: Update DEVICE ORDER INFORMATION

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ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT1270FQAR	Tape & Reel	3000	1270	11	11-

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VIN	9	Power supply input. Must be locally bypassed with a capacitor as close as possible to the pin.
BOOT	10	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW node.
SW	11	Switching node of the boost converter.

K HF F G HI K MBG HG BMBHGL

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.7	12	V
V_{OUT}	Output voltage range	4.5	12.6	V
T_J	Operating junction temperature	-40	150	°C

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PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(2)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

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PARAMETER	THERMAL METRIC	QFN-11L	UNIT
R	Junction to ambient thermal resistance(1)	53.4	°C/W
R	Junction to case thermal resistance(1)	59.2	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT1270 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT1270. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

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V_{IN}=3.6V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		12	V
V_{OUT}	Output voltage range		4.5		12.6	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		2.5 200		V mV
I_{SD}	Shutdown current	EN=0, no load and measured on VIN pin		1		uA
I_Q	Quiescent current from VIN	EN=2V, no load, no switching		1.8		uA
	Quiescent current from VOUT			150		uA
V_{CC}	Internal linear regulator	I_{VCC}=5mA, V_{IN}=6V		4.75		V
V_{CC_UVLO}	VCC UVLO threshold	V_{IN} falling		2.2		V
Reference and Control Loop						
V_{REF}	Reference voltage of FB		0.98	1	1.02	V
I_{FB}	FB pin leakage current	V_{FB}=1V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V		200		uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V		24		uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V		24		uA
V_{COMP_H}	COMP high clamp	V_{FB}=0.8V, R_{ILIM}=100		2.2		V
V_{COMP_L}	COMP low clamp	V_{FB}=1.2V, R_{ILIM}=100 , PFM		0.9		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			17		
R_{DSON_L}	Low side FET on-resistance			14		
Current Limit						
I_{LIM}	Peak current limit	R_{ILIM}=100	7.2	8	8.8	A
		R_{ILIM}=84		9.5		A
Enable						
V_{EN}	Enable high threshold Enable low threshold		 0.4		1.2	V V
R_{EN}	Enable pull down resistance			750		
T_{SS}	Soft-start Current			4		ms
Switching Frequency						
F_{SW}	Switching frequency	R_{FSW}=308 , V_{OUT}=12V		500		kHz
t_{ON_MIN}	Minimum on-time	R_{FSW}=308 $_{OUT}$=12V		170		ns
Protection						
V_{OVP_VOUT}	Output overvoltage threshold Hysteresis	VOUT rising		13.2 280		V mV
T_{SD}	Thermal shutdown threshold	T_J rising		164		°C
	Hysteresis			24		°C

*Derived from bench characterization

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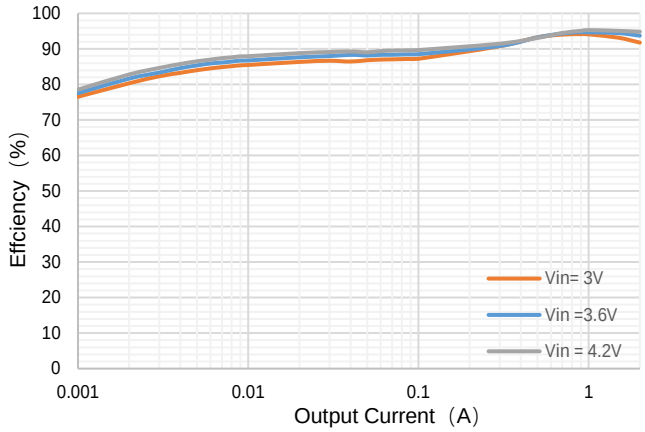

Figure 1. SCT1270 Efficiency vs Load Current, Vout=9V

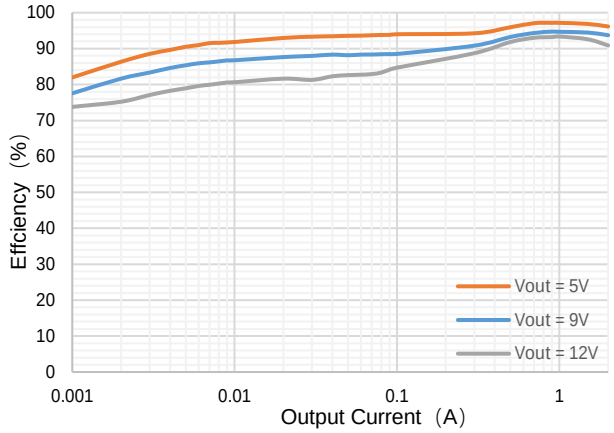

Figure 2. SCT1270 Efficiency vs Load Current, Vin=3.6V

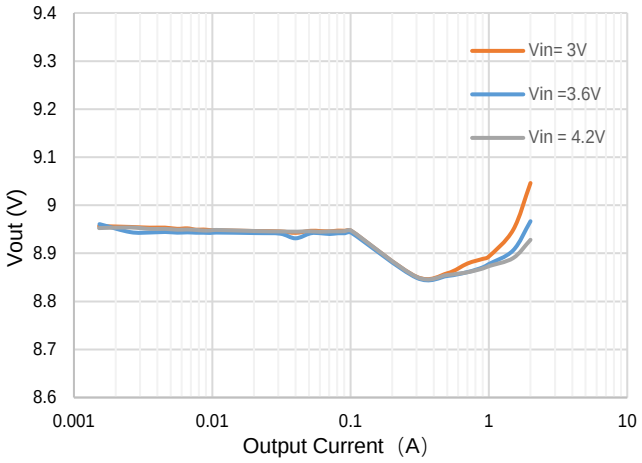

Figure 3. Load Regulation (Vin=3.6V, Vout=9V)

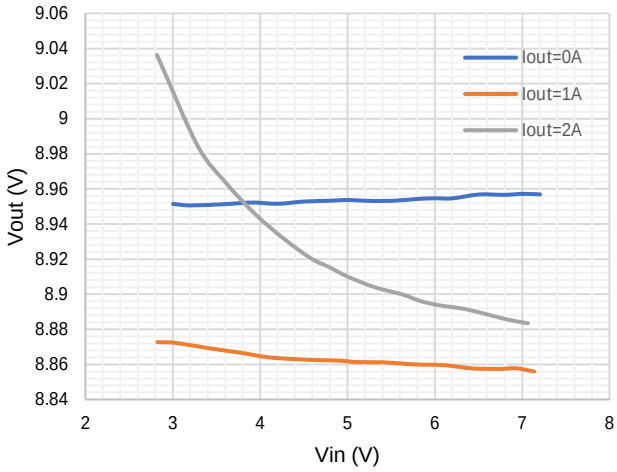

Figure 4. Line Regulation, Vout=9V

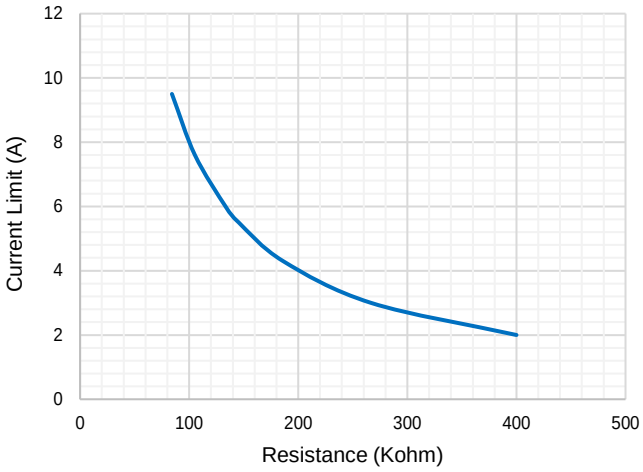

Figure 5. Current Limit VS Setting Resistance

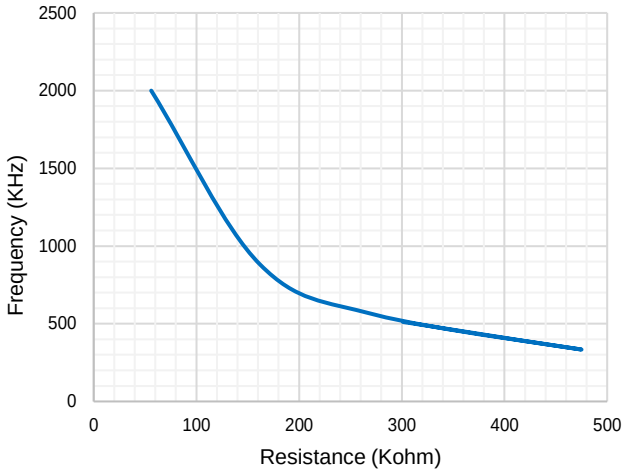

Figure 6. Switching Frequency VS Setting Resistance

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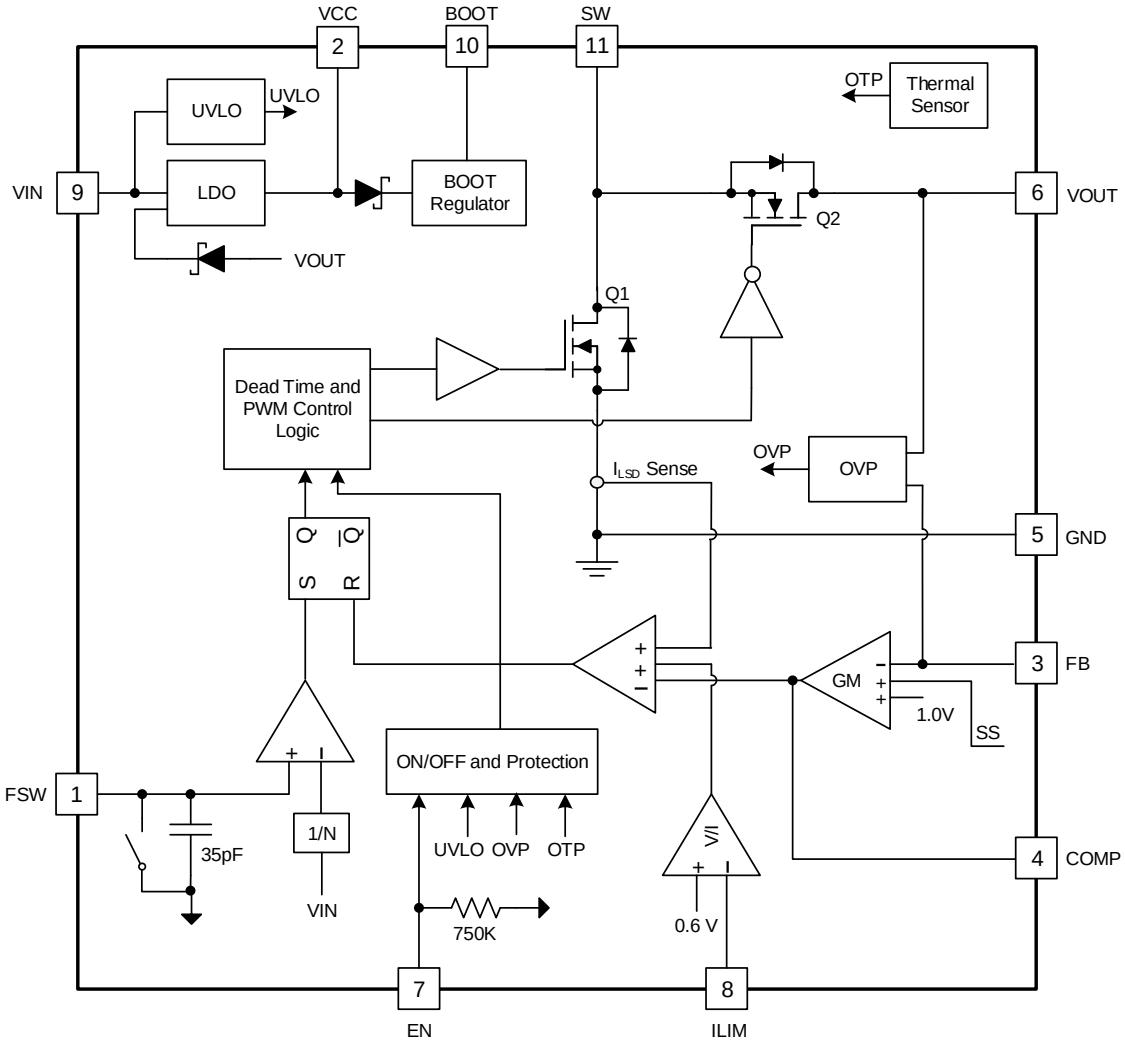

Figure 7. Functional Block Diagram

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Overview

The SCT1270 device is a fully integrated synchronous boost converter, which regulates output voltage higher than input voltage. The constant off-time peak current mode control provides fast transient with pseudo fixed switching frequency. When low-side MOSFET Q1 turns on, input voltage forces the inductor current rise. Sensed voltage on low-side MOSFET peak current rises above the voltage determined by COMP. After the inductor current reaches the peak current, the device turns off low-side MOSFET and inductor goes through body diode of high-side MOSFET Q2 during dead time. After dead time duration, the device turns on high-side MOSFET Q2 and the inductor current decreases. Based on Vin and Vout voltage, the device predicts required off-time and turns off high-side MOSFET Q2. This repeats on cycle-by-cycle based.

The voltage feedback loop regulates the FB voltage to an internal voltage reference with an integrated trans-conductance error amplifier. The feedback loop stability and transient response are optimized through an external loop compensation network connected to the COMP pin.

The SCT1270 works at PFM mode to further increase the efficiency in light load condition. The quiescent current of SCT1270 is 150uA typical under no-load condition and not switching. Disabling the device, the typical supply shutdown current on VIN pin is 1

A resistor connected between SW pin and the FSW pin sets the switching frequency. The wide switching frequency range of 200 kHz to 2.2 MHz offers optimization on efficiency or size of filter components.

The SCT1270 device features internal soft-start, cycle-by-cycle low-side FET current limit, over-voltage protection, and over-temperature protection.

The SCT1270 uses the thermal pad as the power ground. Power ground must be connected to the thermal pad on the PCB at the closest point.

VIN Power

The SCT1270 is designed to operate from an input voltage supply range between 2.7 V to 12V. If the input supply is located more than a few inches from the converter, additional bulk capacitance is required in addition to the ceramic bypass capacitors. A typical choice is ceramic or 2 x 22uF.

VCC Power

The internal VCC LDO provides the bias power supply for internal circuitries. A ceramic capacitor of no less than 1uF is required to bypass from VCC pin to ground. During starting up, input of VCC LDO is from VIN pin. Once the output voltage at VOUT pin exceeds VIN voltage, VCC LDO switches its input to VOUT pin. This allows higher voltage headroom of VCC at lower input voltage. The maximum current capability of VCC LDO is 130mA typical. No additional components or loading are recommended on this pin.

Under Voltage Lockout UVLO

The SCT1270 features UVLO protection for voltage rails of VIN, VCC and BOOT-SW from the converter malfunctioning and the battery over discharging. The default VIN rising threshold is 2.5V typical at startup and falling threshold is 2.3V typical at shutdown. The internal VCC LDO dropout voltage is about 100mV and the device is disabled when VCC falling trips 2.2V typical threshold. The internal charge pump from BOOT to SW powers the gate driver to high-side MOSFET Q2. The BOOT UVLO circuit monitors the capacitor voltage between BOOT pin and SW pin. When the voltage of BOOT to SW falls below a preset threshold 3V typical, high-side MOSFET Q2 turns off. As a result, the device works as a non-synchronous boost converter.

Enable and Start-up

When applying a voltage higher than the EN high threshold (maximum 1.2V), the SCT1270 enables all functions and starts converter operation. To disable converter operation, EN voltage needs fall below its lower threshold

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(minimum 0.4V). An internal 75 the ground. Floating EN pin automatically disables the device.

The SCT1270 features fixed 4ms soft start to prevent inrush current during power-up.

Adjustable Peak Current Limit

The SCT1270 boost converter implements cycle-by-cycle peak current limit function with sensing the internal low-side power MOSFET Q1 during overcurrent condition. While the Q1 is turned on, its conduction current is monitored by the internal sensing circuitry. Once the low-side MOSFET Q1 current exceeds the limit, it turns off immediately. An external resistor connecting ILIM pin to ground sets the low-side MOSFET Q1 peak current limit threshold. Use Equation 1 or Figure 5 to calculate the peak current limit.

$$+\hat{A}\hat{A}\hat{A}\hat{E}\#;\ L\frac{z\ r\ r}{4\hat{A}\hat{A}\hat{A}\hat{E}G\ x;} \quad (1)$$

where:

-

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Typical Application

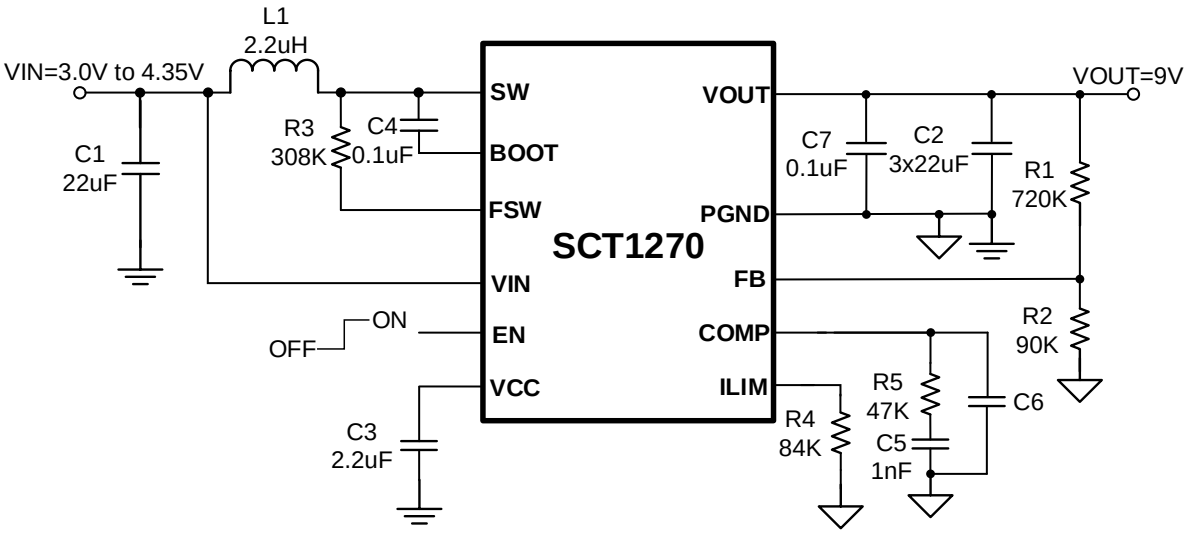

Figure 8. One Cell Battery Input, 9V/2A (20W) Output

Design Parameters

Design Parameters	Example Value
Input Voltage	3.0V to 4.35V
Output Voltage	9V
Output Current	2A
Output voltage ripple (peak to peak)	100mV
Switching Frequency	500 kHz
Operation Mode	PFM

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Switching Frequency

The resistor connected from FSW to SW sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation 3. High frequency can reduce the inductor and output capacitor size with the tradeoff of more thermal dissipation and lower efficiency.

$$4_{¿ Ë ¾ Ê} L \frac{x Û: \frac{5}{Ù Ä È} F 6_{½ ¾ Å ° Ù} \frac{Ï À Æ Å}{Ï ° ¿}}{\%_{¿ Ë ¾ Ê}} \quad (3)$$

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 70 ns
- C_{FREQ} = 35 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

F_{SW}	R_{FREQ}
200 KHz	830
350 KHz	46
520 KHz	300
850 KHz	162
1000 KHz	140
2000 KHz	55

Peak Current Limit

Using the correct external resistor at ILIM pin sets the peak input current. Table 2 shows the resistor value for inductor peak current limit. For a typical current limit of 9.5A, the resistor value is 84 . The minimum current limit must be higher than the required peak switch current at lowest input voltage and the highest output power not to hit the current limit and still regulate the output voltage.

$$+_{Å Â Æ} ;\# ; L \frac{z r r}{4_{Å Â Æ} ;G x} \quad (4)$$

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance of ILIM pin to ground

I_{LIM}	R_{LIM}
9.5 A	84
8 A	100
5.6A	142
4A	200

Output Voltage

The output voltage is set by an external resistor divider R3 and R4 in typical application schematic. A minimum current of typical 20uA flowing through feedback resistor divider gives good accuracy and noise covering. The value of R3 can be calculated by equation 5.

$$4_5 L \frac{: 8_{Ë Î Í} F 8_{Ë ¾ ¿} ; H 4_6}{8_{Ë ¾ ¿}} \quad (5)$$

where:

- V_{REF} is the feedback reference voltage, typical 1.0V

V_{OUT}	R_1	R_2
5 V	360	90
9 V	720	90
12 V	990	90

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Inductor Selection

The performance of
and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

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calculations and bench evaluation. In this application, the Wurth-Elektronix 's inductor 744313220 is used on SCT1270 evaluation board.

Table 4. Recommended Inductors

Part Number	L (uH)	DCR Max	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
744325180	1.8	3.5	18 / 14	10.5 x 10.2 x 4.7	Wurth Elektronix
744311150	1.5	7.2	14 / 11	7.3 x 7.2 x 4.0	Wurth Elektronix
744311220	2.2	12.5	13 / 9	7.3 x 7.2 x 4.0	Wurth Elektronix
744313220	2.2	5.7	18 / 14	12.9 x 12.8 x 3.3	Wurth Elektronix
CDMC8D28NP-1R8MC	1.8	12.6	9.4 / 9.3	9.5 x 8.7 x 3.0	Sumida

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A 0.1 recommended to be placed as close as possible to the VIN pin of the SCT1270. A ceramic capacitor of more than 1.0 internal LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, 2x 22 input capacitance is recommended for most applications. Choose the right capacitor value carefully by

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Loop Stability

An external loop compensation network comprises resister R5, ceramic capacitors C5 and C6 connected to the COMP pin to optimize the loop response of the converter. The power stage small signal loop response of constant off time with peak current control can be modeled by equation 11.

$$)\,É\,Ì\,:5;\ L\,\frac{4_{ß\,â\,Ô\,x}\,H\,:s\,F\,\&;}{t\ H\,4_{Ì\,¾\,Ç\,Ì\,¾}}\ H\,\frac{:s\,E\,\frac{Ì}{6\ HÙ_{Ì\,Ä\,Ã\,Ë}};\,:s\,E\,\frac{Ì}{6\ HÙ_{Ã\,¹\,Á\,Ë}};}{s\,E\,\frac{Ì}{6\ HÙ_{Á}}} \tag{11}$$

where

- D is the switching duty cycle.
- R_{load} is the output load resistance.
- R_{SENSE} is the equivalent internal current sense resistor, which is 0.14

$$B_{Ë}\ L\,\frac{s}{t\,è\,H\,4_{ß\,â\,Ô\,x}\,H\,\%_{Ë}} \tag{12}$$

where

- C_O is the output capacitance

$$B_{Ë\,¾\,Ì\,Ë\,Ó}\ L\,\frac{s}{t\,è\,H\,'\,5\,4\,H\,\%_{Ë}} \tag{13}$$

where

- ESR is the equivalent series resistance of the output capacitor.

$$B_{Ë\,Á\,É\,Ó}\ L\,\frac{4_{ß\,â\,Ô\,x}\,H\,:s\,F\,\&;^{6}}{t\,è\,H\,.} \tag{14}$$

The COMP pin is the output of the internal trans-conductance amplifier. Equation 15 shows the small signal transfer function of compensation network.

$$)\,_{¼}:5;\ L\,\frac{)\,_{¾\,º}\,H\,4_{¾\,º}\,H\,8_{Ë\,¾\,¿}}{8_{Ë\,Î\,Í}}\ H\,\frac{:s\,E\,\frac{Ì}{6\ HÙ_{À\,¾\,Ë}};}{:s\,E\,\frac{Ì}{6\ HÙ_{À\,¾\,Á}};\,:s\,E\,\frac{Ì}{6\ HÙ_{À\,¾\,Á}};} \tag{15}$$

where

- G_{EA} -conductance
- R_{EA}
- V_{REF} is the reference voltage at the FB pin
- V_{OUT} is the output voltage
- $_{COMP1}$ $_{COMP2}$ are the poles' frequency of the compensation network.
- $_{COMZ}$ is the zero's frequency of the compensation network.

$_{C}$. The higher frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/1 $_{SW}$ $_{RHPZ}$.

Then set the value of R5, C8, and C9 in typical application circuit by following these equations.

$$4_{9}\ L\,\frac{t\,è\,H\,8_{Ë\,Î\,Í}\ H\,4_{Ì\,¾\,Ç\,Ì\,¾}\,H\,B_{¾}\,H\,\%_{Ë}}{:s\,F\,\&;\ H\,8_{Ë\,¾\,¿}\,H\,)\,_{¾\,º}} \tag{16}$$

where

- $_{C}$ is the selected crossover frequency.

$$\%_{9}\ L\,\frac{4_{ß\,â\,Ô\,x}\,H\,\%_{Ë}}{t\ H\,4_{9}} \tag{17}$$

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$$\% \; L \frac{' 5 \; 4 \; H \; \%_{E}}{4_{9}} \tag{18}$$

If the calculated value of C6 is less than 10pF, it can be left open. Designing the loop for greater than 45°of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

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Application Waveforms

Vin=3.6V, Vout=9V, unless otherwise noted

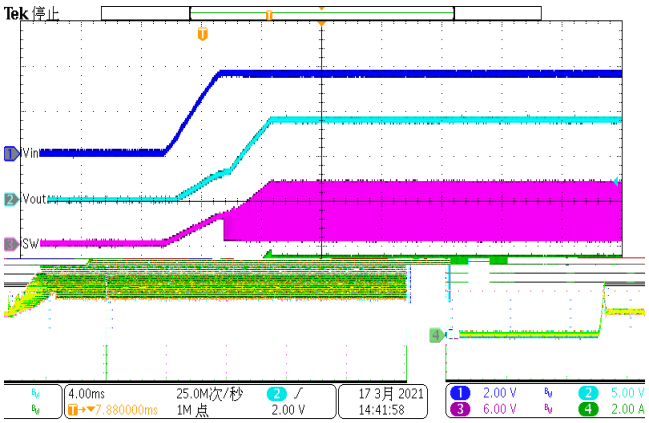

Figure 9. Power up

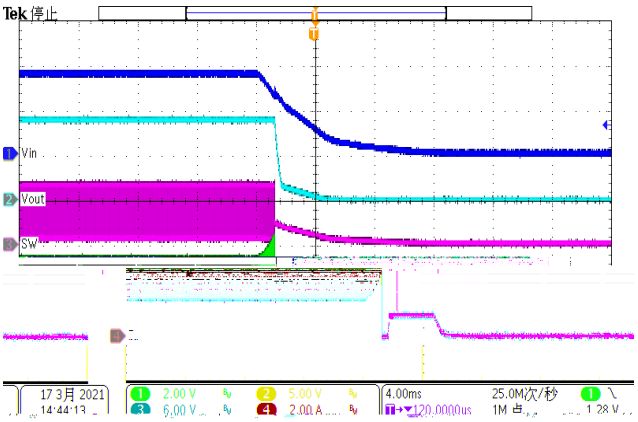

Figure 10. Power down

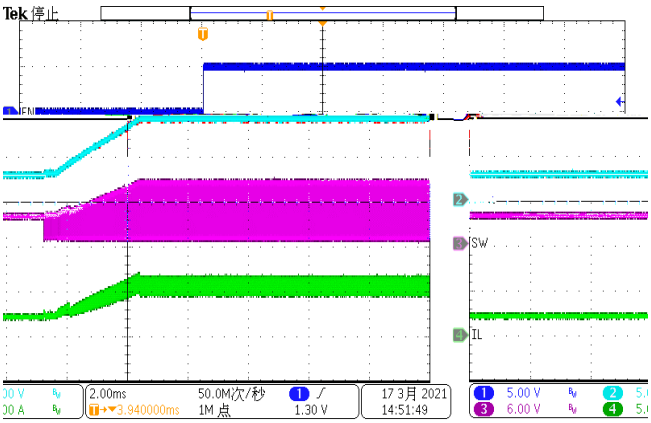

Figure 11. EN Power up (Iload=2A)

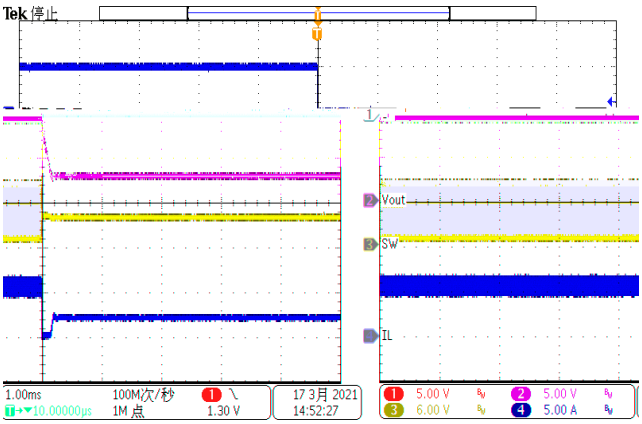

Figure 12. EN Power down(2A)

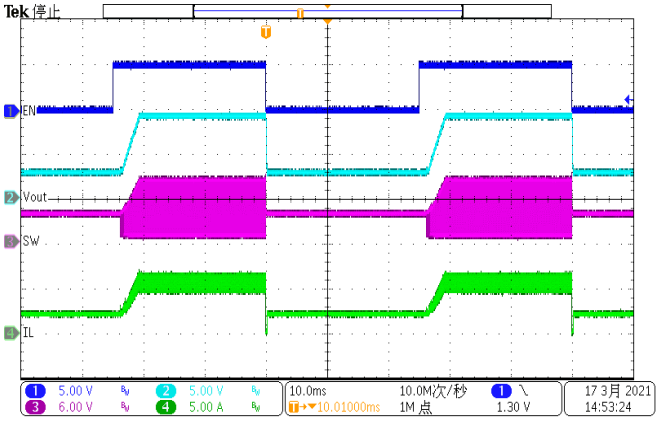

Figure 13. EN toggle (Iload=2A)

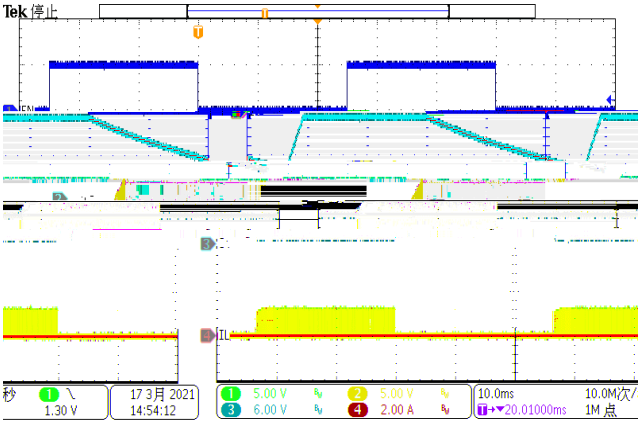

Figure 14. EN toggle (Iload=10mA)

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Application Waveforms(continued)

Vin=3.6V, Vout=9V, unless otherwise noted

Figure 15. Load transient (0.2A-1.8A, 1.6A/us)

Figure 16. Load transient

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Layout Guideline

The regulator could suffer from instability and noise problems without careful layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be close to the VIN pin and ground pad to reduce the input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier FET, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the VOUT pin, but also to the GND pin to reduce the overshoot at the SW pin and VOUT pin. The placement and ground trace for output capacitor is critical for the performance of SW ringing voltage. Place the 0.1uF output capacitor as close to VOUT pins and power ground pad as possible to reduce high frequency ringing voltage on SW pin.

The layout should also be done with well consideration of the thermal. The SW, VOUT and GND pad under the chip should always be soldered well to the board for thermal, mechanical strength and reliability. Improper soldering will cause SW higher ringing and overshoot besides downgrading thermal performance.

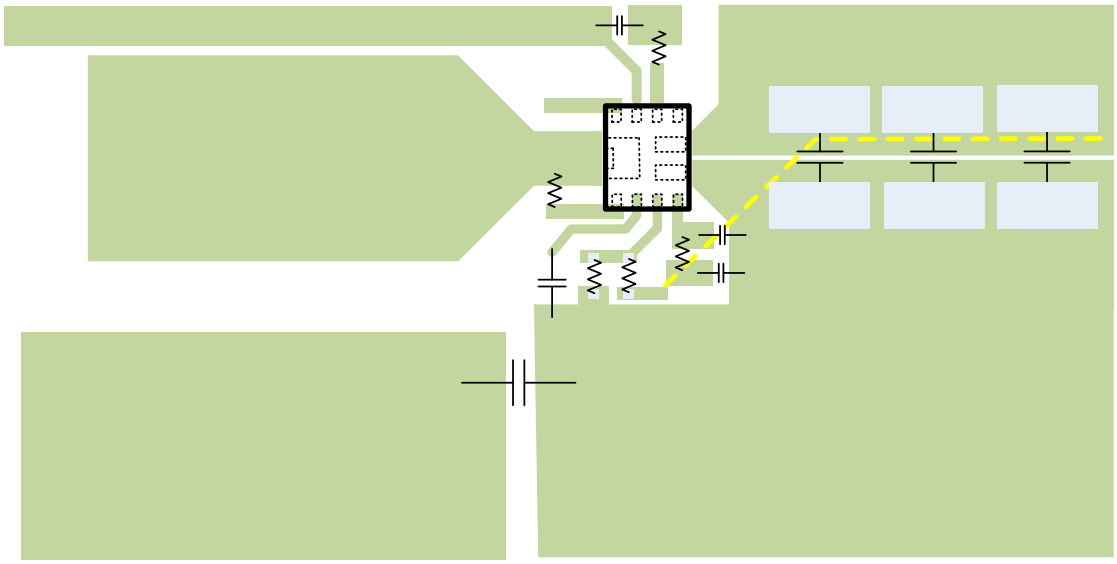

Figure 21. PCB Layout Example Top Layer

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Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 19.

$$2\frac{\text{½:ÆºÑ}}{} L \frac{\text{s w IF 6 \%}}{4\text{~ N E}} \quad (19)$$

where

- T_A is the maximum ambient temperature for the application.
- R is the junction-to-ambient thermal resistance given in the Thermal Information table.

SCT1270 QFN package includes a thermal pad that improves the thermal capabilities of the package. The real junction-to-ambient thermal resistance R of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

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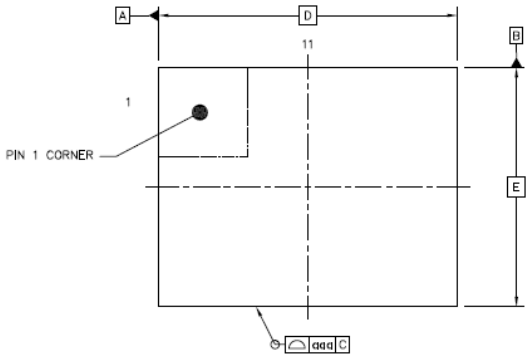
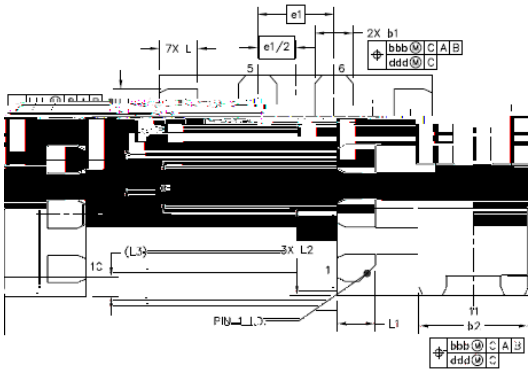
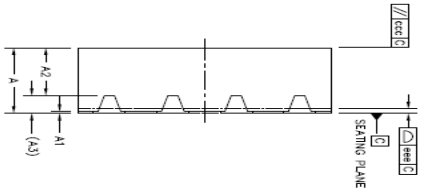
I D BG HKF MBHG



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	---	0.55	---
A3		0.203 REF	
b	0.20	0.25	0.30
b1	0.30	0.35	0.40
b2	0.95	1	1.05
D		2.5 BSC	
E		2 BSC	
e		0.5 BSC	
e1		0.7 BSC	
L	0.3	0.35	0.4
L1	0.25	0.35	0.45
L2	0.75	0.8	0.85
L3		0.18 REF	
aaa		0.1	
ccc		0.1	
eee		0.05	
bbb		0.1	
ddd		0.05	

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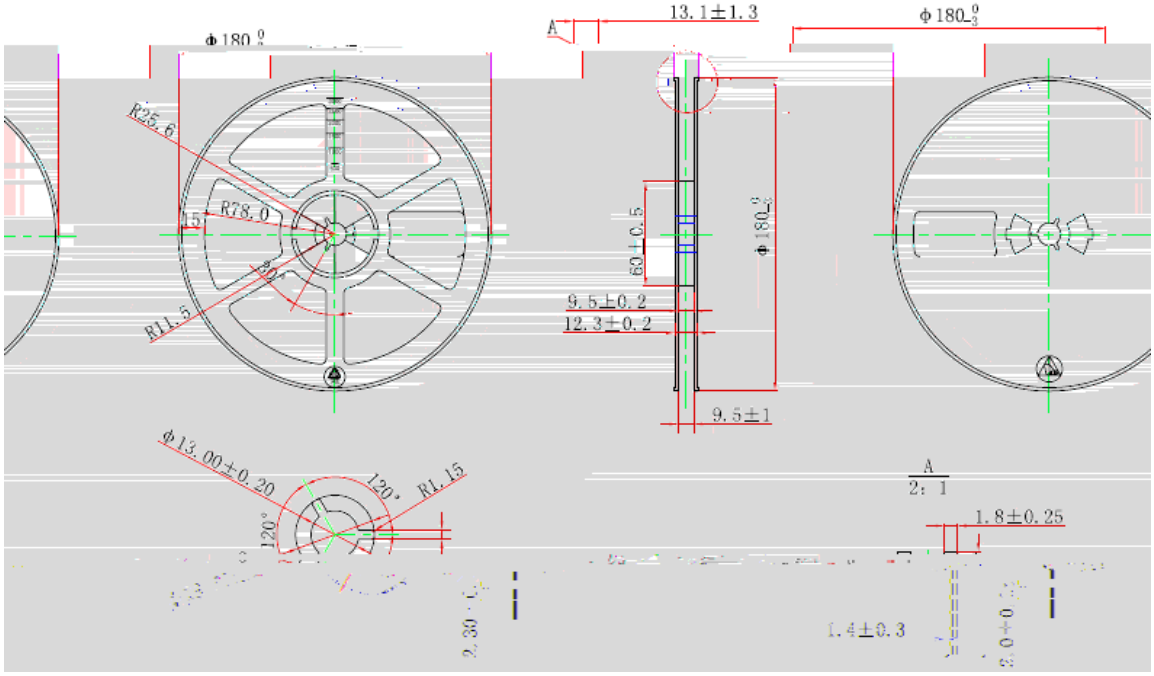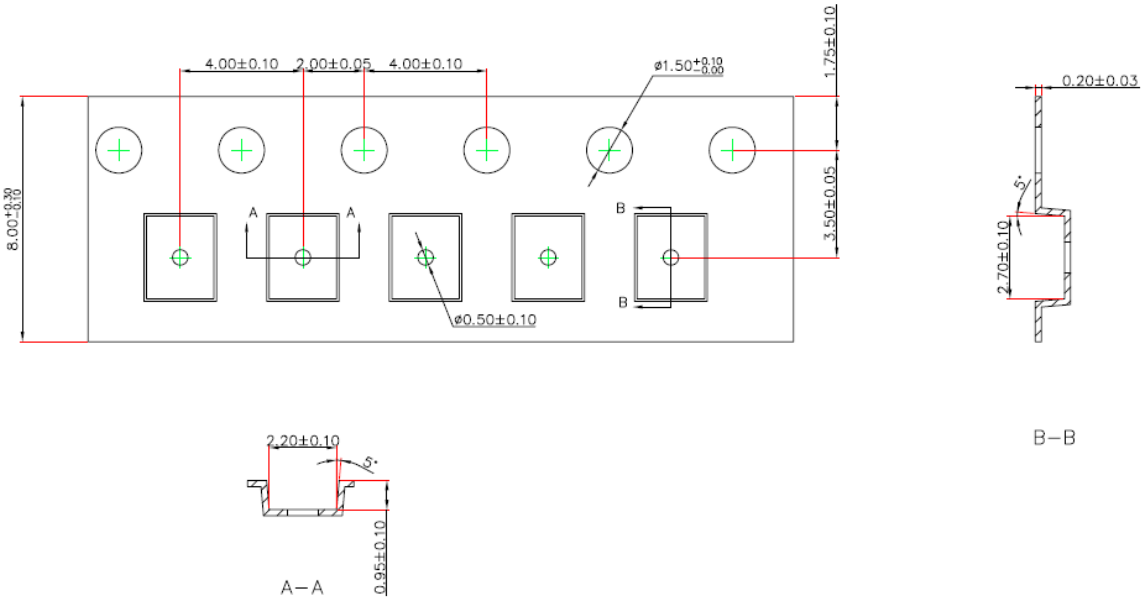
M I G K E BG HKF MBHG