REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production.

Revision 1.1: Format adjustment, update ABS max, add EC table max limit

Revision 1.2: Correct package information in Page 16

Revision 1.3: Update DEVICE ORDER INFORMATION

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT52242STDR	Tape & Reel	4000	2242	8	SOP-8L

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION MIN M C q 2

PIN CONFIGURATION

Top View: SOP-8pin

 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	4.5	24	V
$V_{INA-,INB-}$	Input voltage range	-5	24	
T_J	Operating junction temperature	-40	150	℃

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV

 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

TYPICAL CHARACTERISTICS

V_{IN}=12V, T_A= 25℃.

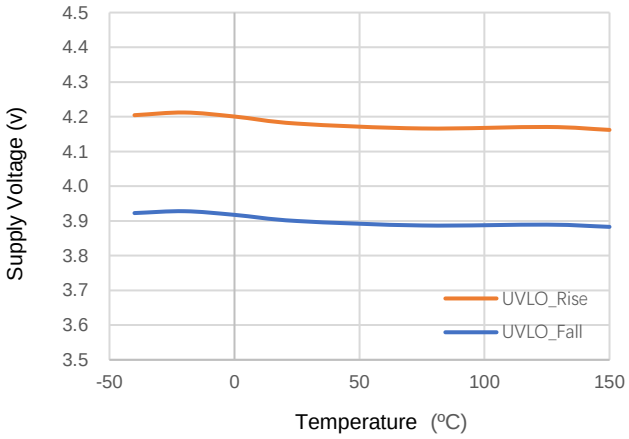


Figure 1. UVLO vs Temperature

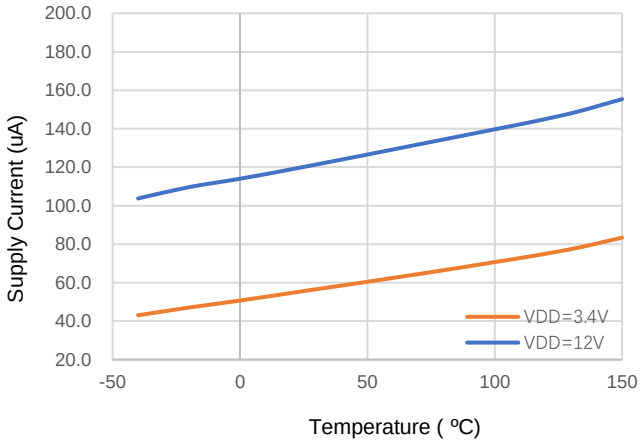


Figure 2. Supply current vs Temperature

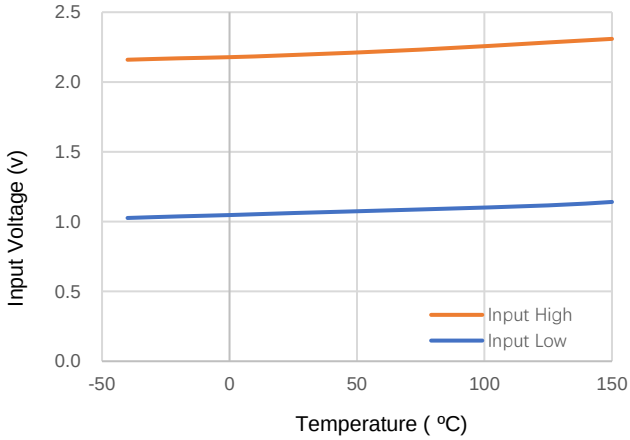


Figure 3. Input Threshold vs Temperature

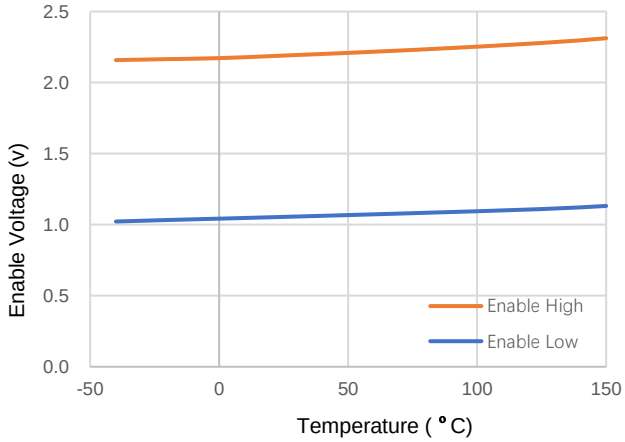


Figure 4. Enable Threshold vs Temperature

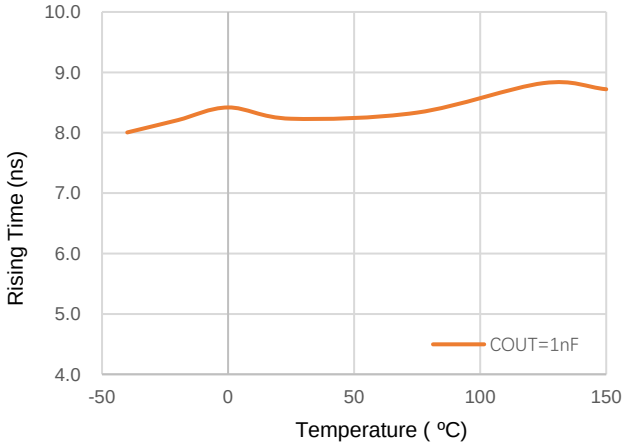


Figure 5 Output Rising Time vs Temperature

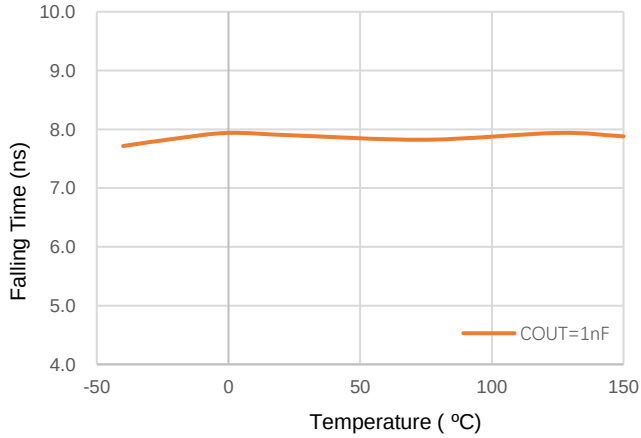


Figure 6. Output Falling Time vs Temperature

 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

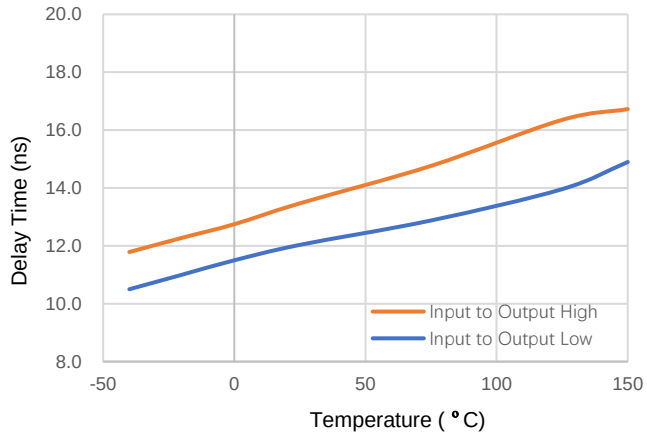


Figure 7. Input to Output Propagation Delay vs Temperature

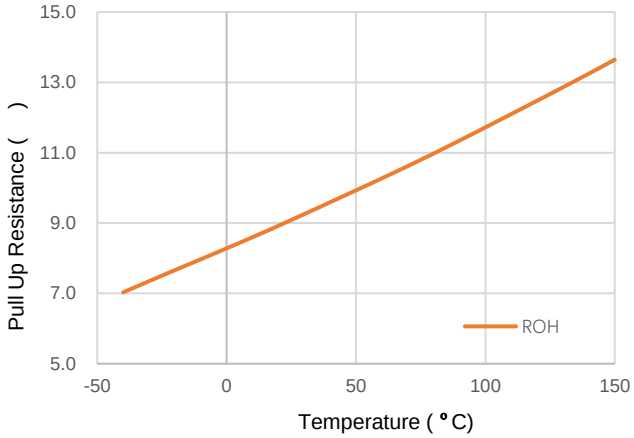


Figure 8. ROH vs Temperature

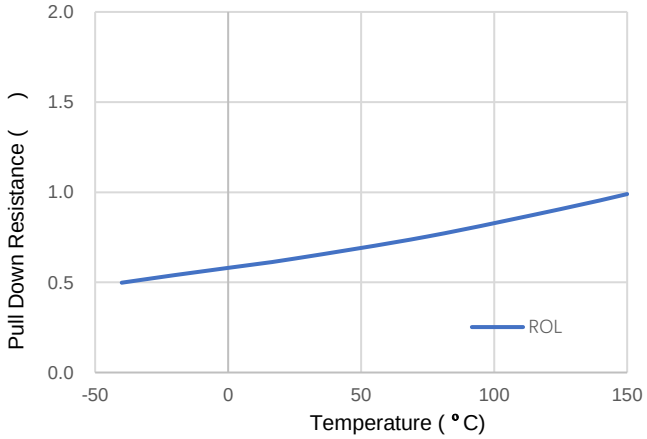


Figure 9. ROL vs Temperature

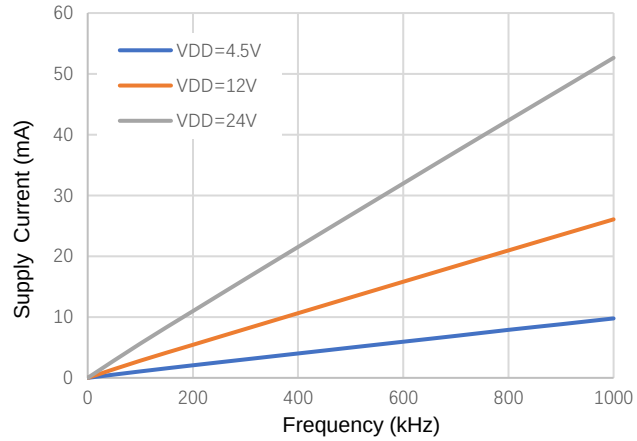
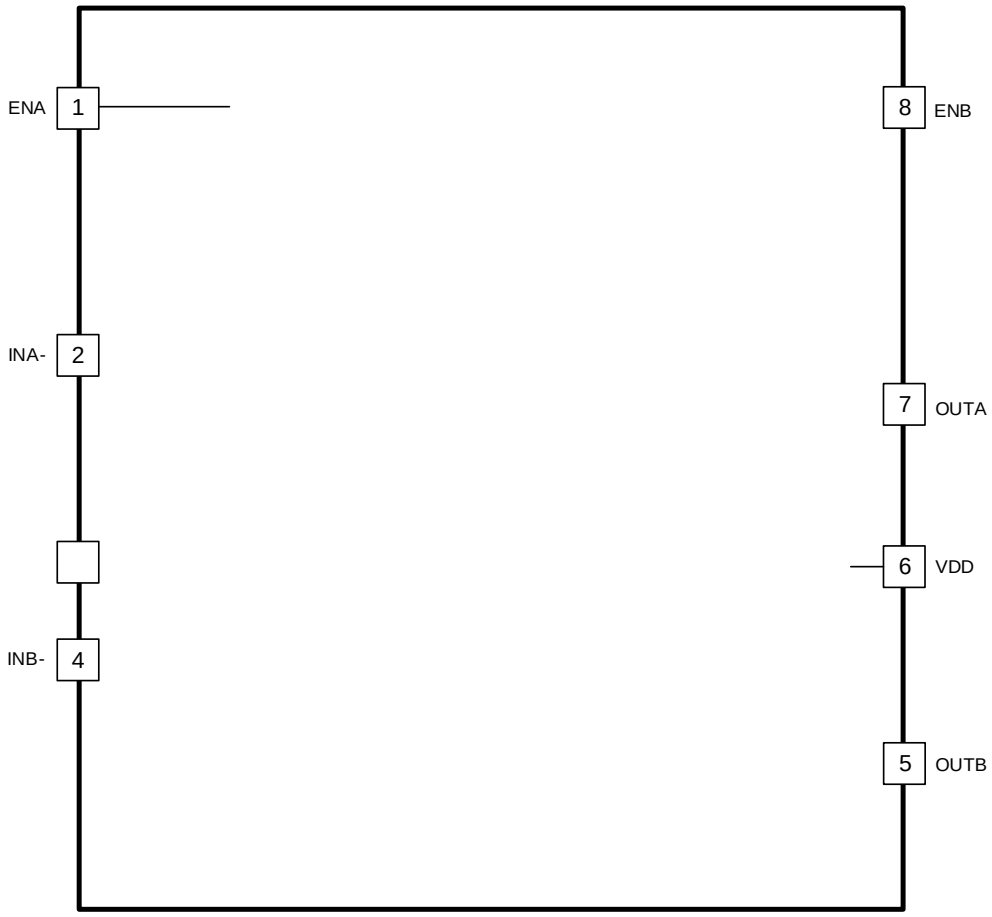


Figure 10. Operation Supply Current vs Frequency, C_{OUT}=1nF

 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

FUNCTIONAL BLOCK DIAGRAM



 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

OPERATION

Overview

The SCT52242 is a dual-channel non-invertible high-speed low side driver with supporting up to 24V wide supply for both power MOSFET and IGBT. Each channel can source and sink 4A peak current along with the minimum propagation delay 13ns from input to output. The 1ns delay matching and the stackable output characteristics support higher driving capability demanding in high power converter application. The ability to handle -5V DC input increases the noise immunity of driver input stage, the 24V rail-to-rail output improves the SCT52242 output stage robustness during switching load fast transition. The SCT52242 has flexible input and enable pin configuration, table 1 shows the device output logic truth table.

. Table 1: the SCT52242 Device Logic.

ENA	ENB	INA-	INB-	OUTA	OUTB
H	H	L	L	H	H
H	H	L	H	H	L
H	H	H	L	L	H
H	H	H	H	L	L
L	L	Any	Any	L	L
Any	Any	Floating	Floating	L	L
Floating	Floating	L	L	H	H
Floating	Floating	L	H	H	L
Floating	Floating	H	L	L	H
Floating	Floating	H	H	L	L

VDD Power Supply

The SCT52242 operates under a supply voltage range between 4.5V to 24V. For the best high-speed circuit performance, two VDD bypass capacitors in parallel are recommended to prevent noise problems on supply VDD. A 0.1- F surface mount ceramic capacitor must be located as close as possible to the VDD to GND pins of the SCT52242. In addition, a larger capacitor (such as 1- F or 10uF) with relatively low ESR must be connected in parallel, in order to help avoid the unexpected VDD supply glitch. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

Under Voltage Lockout (UVLO)

SCT52242 device Under Voltage Lock Out (UVLO) rising threshold is typically 4.2 V with 300-mV typical hysteresis. When VDD is rising and the level is still below UVLO threshold, this circuit holds the output low regardless of the status of the inputs. The hysteresis prevents output bouncing when low VDD supply voltages have noise from the power supply. The capability to operate at low voltage below 5 V, is especially suited for driving new emerging wide band gap power device like GaN. For example, at power up, the driver output remains low until the VDD voltage reaches the UVLO threshold if enable pin is active or floating. The magnitude of the OUT signal rises with VDD until steady state VDD reached.

The inverting operation in Figure 11 shows that the output remains low until the UVLO threshold reached, and then the output is Out-of-phase with the input.

 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

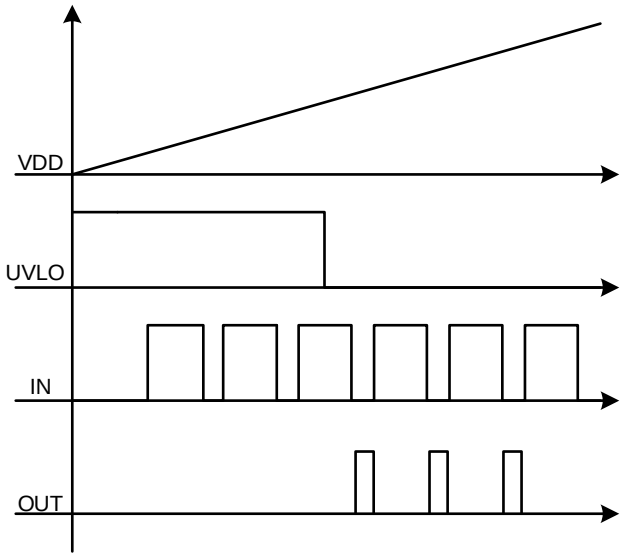


Figure 11. SCT52242 Output Vs VDD

Enable Function

SCT52242 provides independent enable pins ENA and ENB for external control of each channel operation. The enable pins are based on a TTL compatible input-threshold logic that is independent of the supply voltage and is effectively controlled with logic signals from 3.3-V and 5-V microcontrollers. When applying a voltage higher than the high threshold (typical 2.1V) the pin, the SCT52242 enables all functions and starts gate driver operation. Driver operation is disabled when ENx

 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

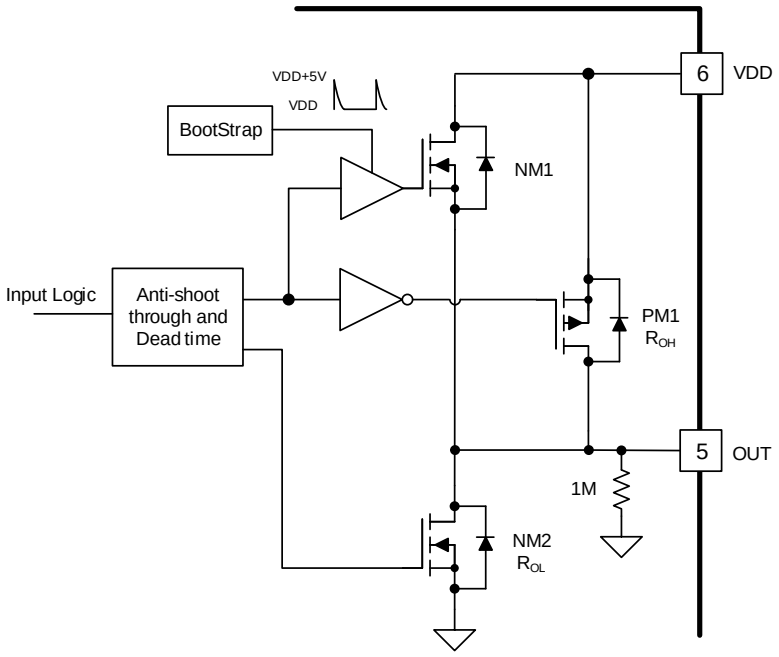


Figure 12. SCT52242 Output Stage

Stackable Output

The SCT52242 features 1ns (typical) delay matching between dual channels, which enables dual channel outputs be stackable when the driven power device required higher driving capability. By using SCT52242, the OUTA and OUTB can be connected together to provide the higher driving capability, so does the INA- and INB-. As a result, a single input signal controls the stacked output combination. To support the stackable output, each channel output stage artificially implements up to 5ns dead-time to avoid the possible shoot-through between two channels as shown Figure 13.

Due to the rising and falling threshold mismatch between INA- and INB-, cautions must be taken when implementing stackable output of OUTA and OUTB together. The maximum mismatch between INA- and INB- input threshold is up to 10mV (maximum cross temperature), as a result the allowed minimum slew rate of input logic signal is 2V/us. The following suggestions are recommended when INA- and INB- connected together and along with the OUTA and OUTB:

1. Apply the fast slew rate dv/dt on input (2 V/us or greater) to avoid the possible shoot-through between OUTA and OUTB output stage.
2. INA- and INB- must be connected as close to the pins as possible.

 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

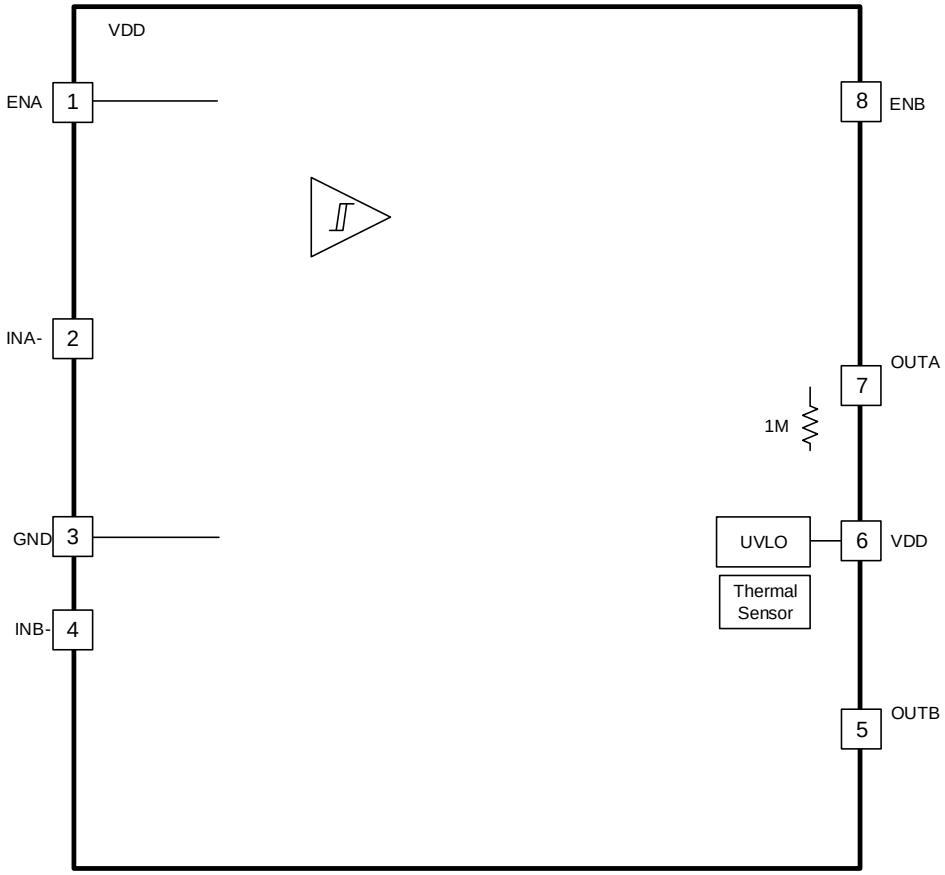


Figure 13. SCT52242 Stackable output

The Figure 14 and Figure 15 shows the stackable output with 2V/us input signal.

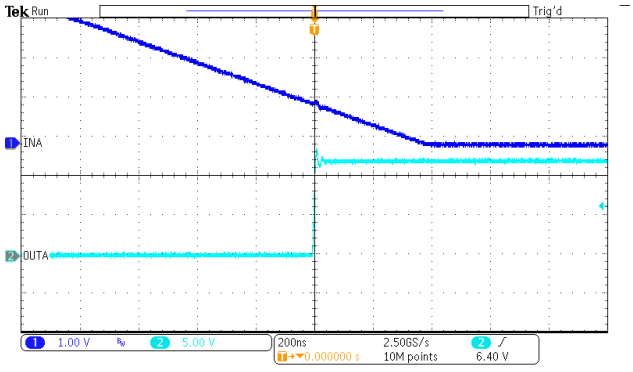


Figure 14. Driver Switching ON

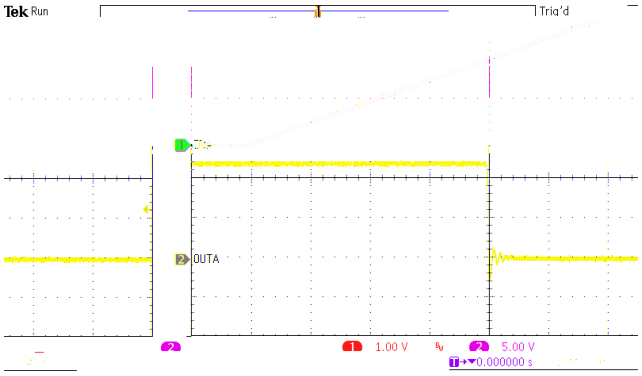


Figure 15. Driver Switching OFF

Thermal Shutdown

Once the junction temperature in the SCT52242 exceeds 170° C, the thermal sensing circuit stops switching until the junction temperature falling below 145° C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application

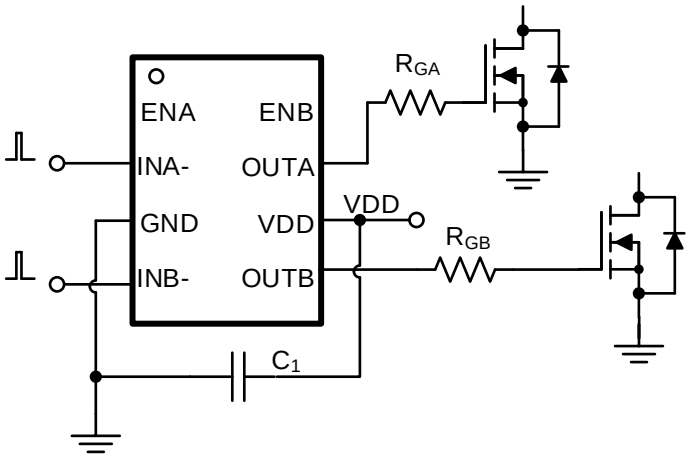


Figure 16. Dual Channel Driver Typical Application

Driver Power Dissipation

Generally, the power dissipated in the SCT52242 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52242 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of each channel in SCT52242 is:

(1)

Where

- V_{DD} is supply voltage
- C_{Load} is the output capacitance
- F_{SW} is the switching frequency

For the the switching load of power MOSFET, the power loss of each channel in the SCT52242 is shown in equation (2), where charging a capacitor is determined by using the equivalence $Q_g = C_{LOAD}V_{DD}$. The gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions.

(2)

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

If R_G applied between driver and gate of power device to slow down the power device transition, the power dissipation of the driver shows as below:

– (——— ———)

(3)

 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

Where

- R_{OH} is the equivalent pull up resistance of SCT52242
- R_{OL} is the pull down resistance of SCT52242
- R_G is the gate resistance between driver output and gate of power device.

 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

Application Waveforms

Figure 17. Driver Switching ON

Figure 18. Driver Switching OFF

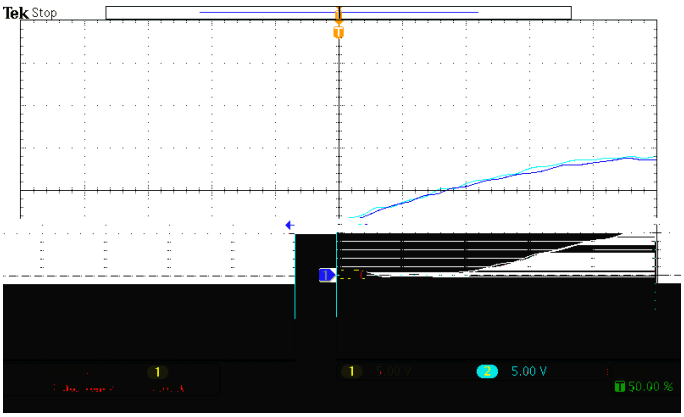


Figure 19. Delay Matching Rise

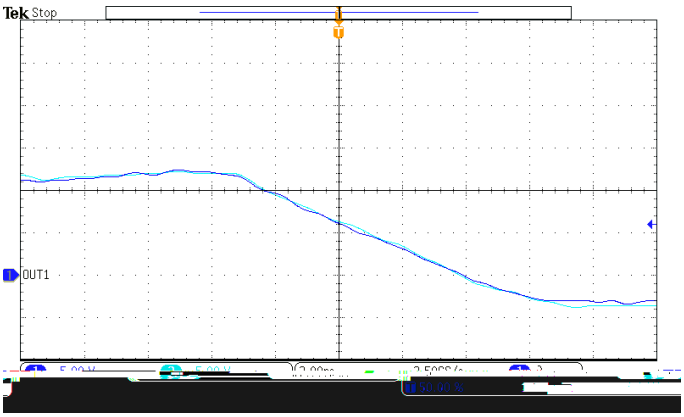


Figure 20. Delay Matching Fall

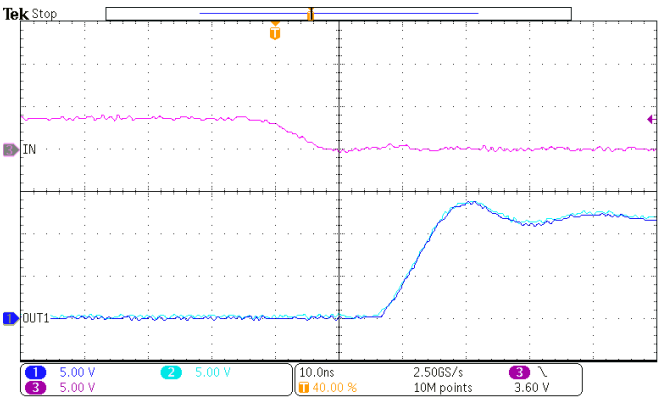


Figure 21. Stackable Output Rise

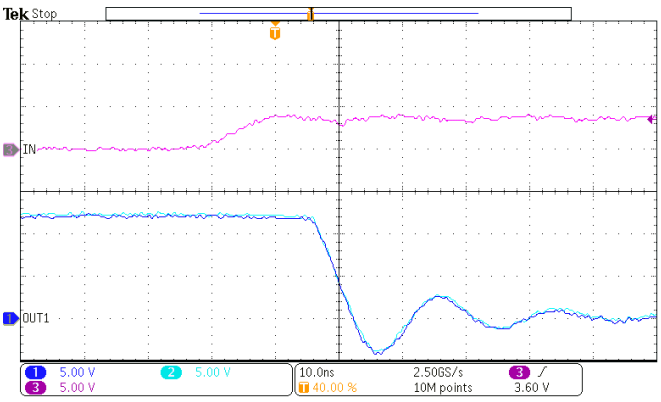


Figure 22. Stackable Output Fall

 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

Layout Guideline

The SCT52242 provides the 4A output driving current and features very short rising and falling time at the power devices gate. The high di/dt causes driver output unexpected ringing when the driver output loop is not designed well. The regulator could suffer from malfunction and EMI noise problems if the power device gate has serious ringing. Below are the layout recommendations with using SCT52242 and Figure 23 is the layout example.

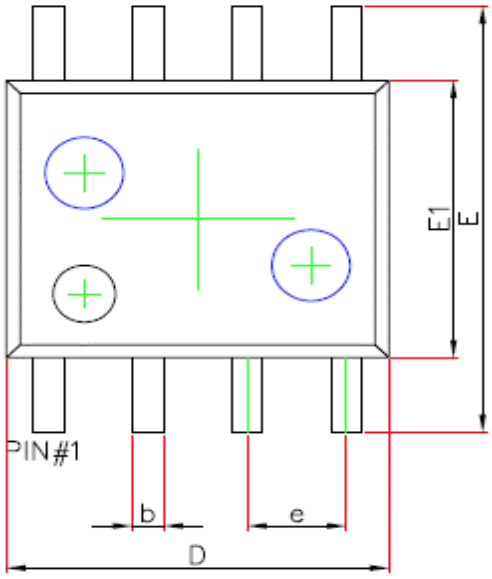
Put the SCT52242 as close as possible to the power device to minimize the gate driving loop including the driver output and power device gate. The power supply decoupling capacitors needs to be close to the VDD pin and GNDID 80/Lang (

 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

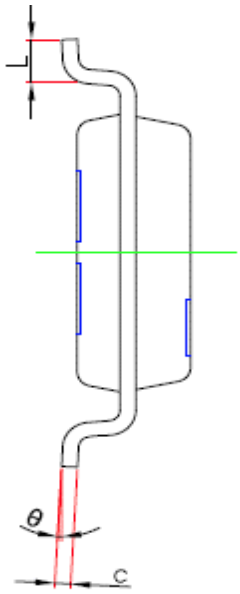
The real junction-to-ambient thermal resistance R $_{\theta JA}$ of the package greatly depends on the PCB type, layout, and environmental factor. Soldering the ground pin to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

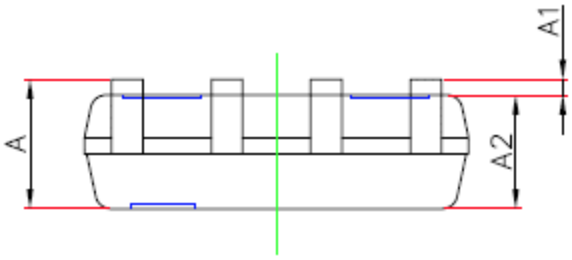
PACKAGE INFORMATION (SOP-8)



TOP VIEW



BOTTOM VIEW

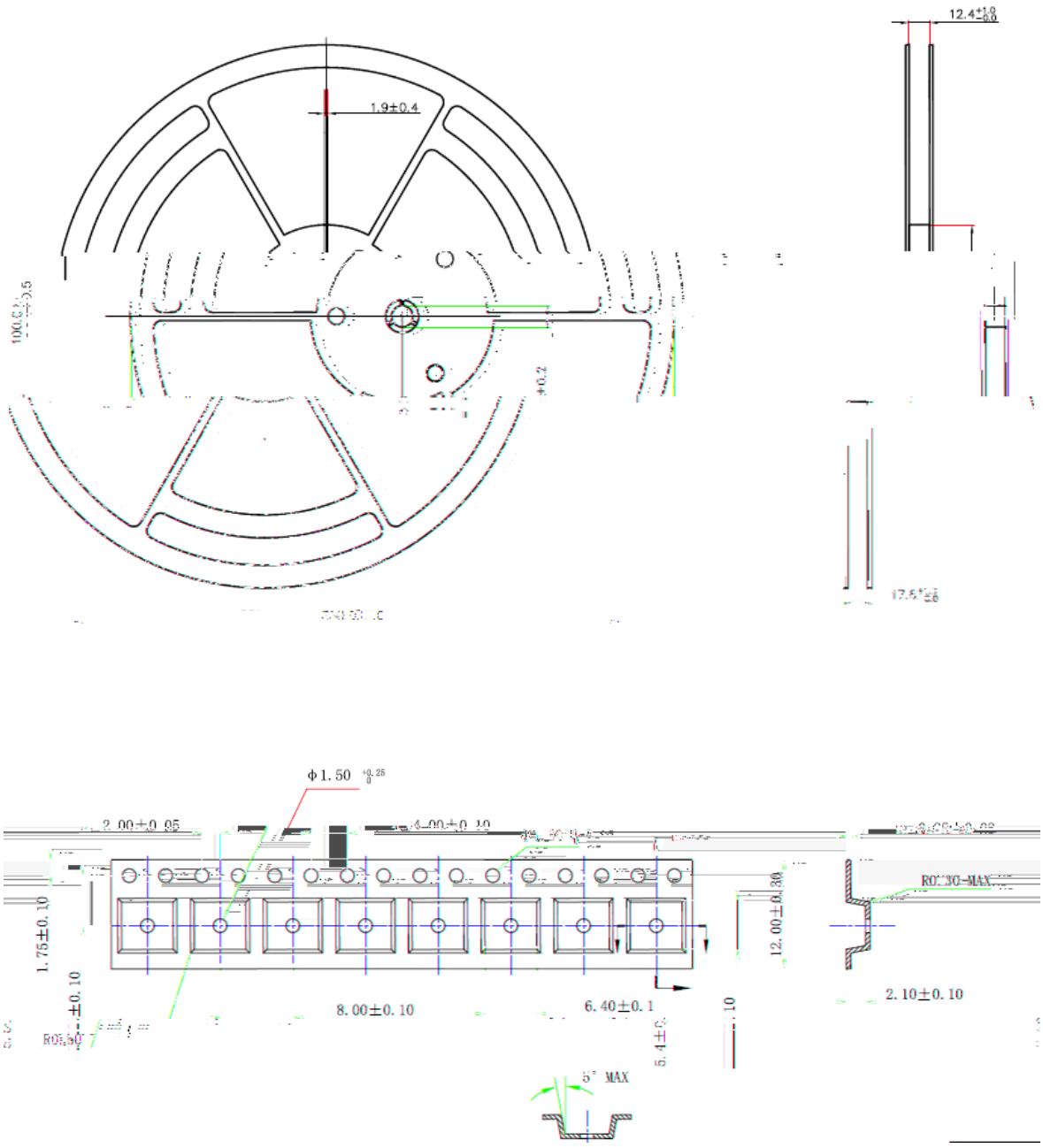


SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	1.45	---	1.75
A1	0.1	---	0.25
A2	1.35	---	1.55
b	0.33	---	0.51
c	0.17	---	0.25
D	4.7		5.1
E	5.8		6.2
E1	3.8		4.0
e	1.27BSC		
L	0.4		1.27
G	0°		8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

 © 2019 Silicon Content Technology Co., Ltd. All Rights Reserved

TAPE AND REEL INFORMATION