NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Production

Revision 1.3: Update package information, ABS max, add EC table max limit

Revision 1.4: Format adjustment

Revision 1.5: Correct package information in Page 16

Revision 1.6: Correct operating junction temperature

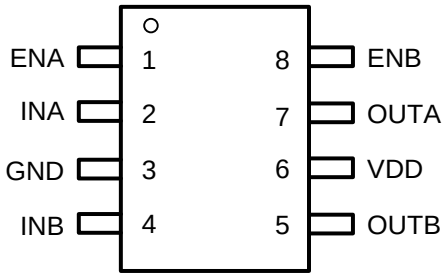
Revision 1.7: Update DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT52240STDR	Tape & Reel	4000	2240	8	SOP-8L
SCT52240MTER	Tape & Reel	4000	2240	8	eMSOP-8L

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
ENA, ENB	-0.3	26	V
INA, INB	-5	26	V
OUTA, OUTB	-0.3	VDD+0.3	V
OUTA, OUTB (Pulse<0.2us)	-3	VDD+3	V
VDD	-0.3	26	V
Operating junction temperature TJ (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

Top View: SOP-8pin
Plastic



(1) Stresses beyond those listed under Absolut Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

NAME	NO.	PIN FUNCTION
ENA	1	Channel A enable logic input, TTL compatible. Floating logic high.
INA	2	Channel A logic input, TTL compatible. Floating logic low.
GND	3	Power ground. Must be soldered directly to ground plane for thermal performance improvement and electrical contact.
INB	4	Channel B logic input, TTL compatible. Floating logic low.
OUTB	5	Channel B gate driver output

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved

VDD	6	Power Supply, must be locally bypassed by the ceramic cap.
OUTA	7	Channel A gate driver output
ENB	8	Channel B enable logic input, TTL compatible. Floating logic high.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	4.5	24	V
$V_{INA,INB}$	Input voltage range	-5	24	
T_J	Operating junction temperature	-40	125	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved

V_{DD}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{DD}	Operating supply voltage		4.5		24	V
V_{DD_UVLO}	Input UVLO Hysteresis	V_{DD} rising		4.2 300	4.5	V mV
I_Q	Supply current	EN=V_{DD}=3.5V, INA=INB=GND		55	115	uA
		EN=V_{DD}=12V, INA=INB=GND		120	190	uA
INPUTS						
V_{INA,INB_H}	Input logic high threshold			2.1	2.4	V
V_{INA,INB_L}	Input logic low threshold		0.8	1		V
V_{IN_Hys}	Hysteresis			1.1		V
V_{ENA,ENB_H}	Enable logic high threshold			2.1	2.4	V
V_{ENA,ENB_L}	Enable logic low threshold		0.8	1		V
V_{EN_Hys}	Hysteresis			1.1		V
OUTPUTS						
V_{DD_VOH}	Output output high voltage	I_{OUT}= - 10mA			150	mV
V_{OL}	Output low voltage	I_{OUT}= 10mA			10	mV
$I_{SINK/SRC}$	Output sink/source peak current(1)	C_{Load}=10nF, F_{SW}=1kHz		4		A
R_{OH}	Output pull high resistance (only PMOS ON)	I_{OUT}= - 10mA	5	9	18	
R_{OL}	Output pull low resistance	I_{OUT}= 10mA	0.3	0.6	1.2	
Timing						
T_R	Output rising time	C_{Load}=1nF		8	20	ns
T_F	Output falling time	C_{Load}=1nF		8	20	ns
T_{D_IN}	Input to output propagation delay, Rising edge		7	13	25	ns
	Input to output propagation delay, Falling edge		7	13	25	ns
T_{M_IN}	Input to output delay matching			1	4	ns
T_{MIN_ON}	Minimum input pulse width	C_{Load}=1nF		20	30	ns
Protection						
T_{SD}	Thermal shutdown threshold	T_J rising		170		°C
	Hysteresis			25		°C

(1)Guaranteed by design

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved

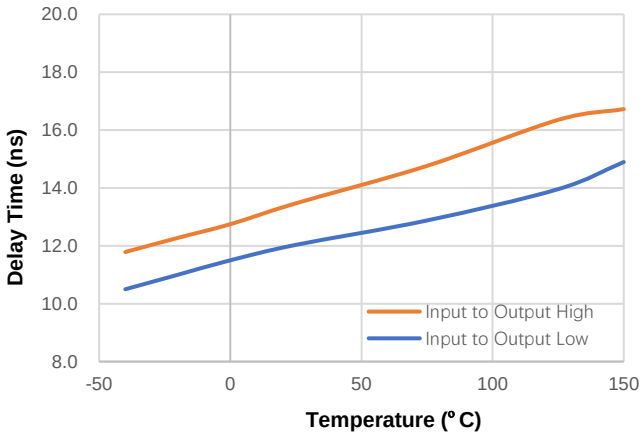


Figure 7. Input to Output Propagation Delay vs Temperature

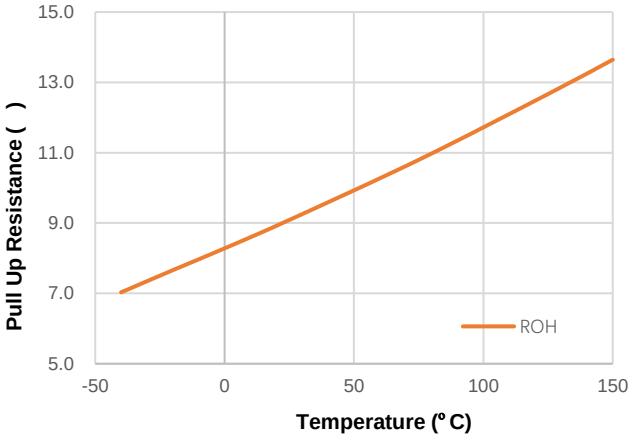


Figure 8. ROH vs Temperature

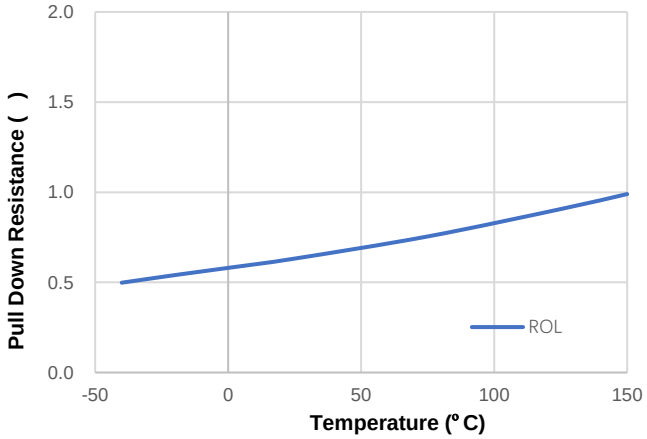


Figure 9. ROL vs Temperature

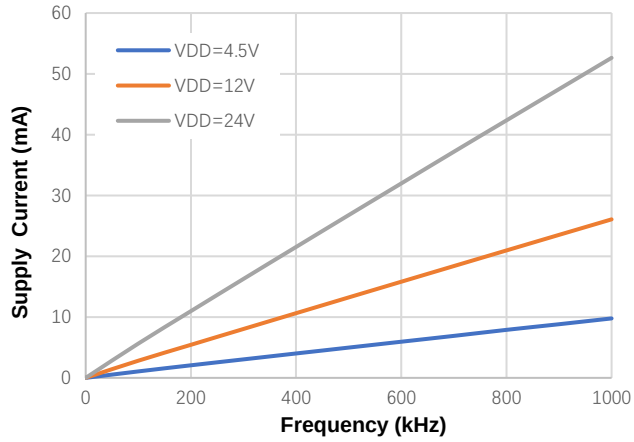
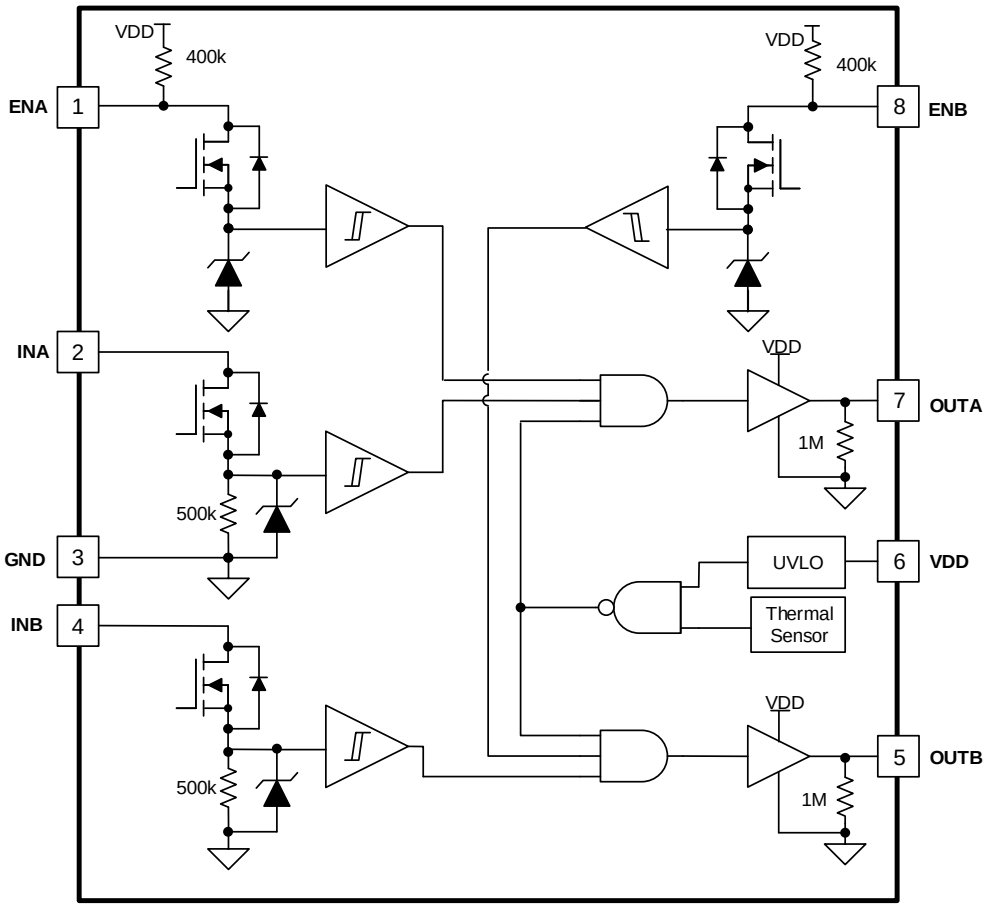


Figure 10. Operation Supply Current vs Frequency, C_{OUT}=1nF

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved



 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved

Overview

The SCT52240 is a dual-channel non-invertible high-speed low side driver with supporting up to 24V wide supply for both power MOSFET and IGBT. Each channel can source and sink 4A peak current along with the minimum propagation delay 13ns from input to output. The 1ns delay matching and the stackable output characteristics support higher driving capability demanding in high power converter application. The ability to handle -5V DC input increases the noise immunity of driver input stage, the 24V rail-to-rail output improves the SCT52240 output stage robustness during switching load fast transition. The SCT52240 has flexible input and enable pin configuration, table 1 shows the device output logic truth table.

. Table 1: the SCT52240 Device Logic.

ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	Floating	Floating	L	L
Floating	Floating	L	L	L	L
Floating	Floating	L	H	L	H
Floating	Floating	H	L	H	L
Floating	Floating				

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved

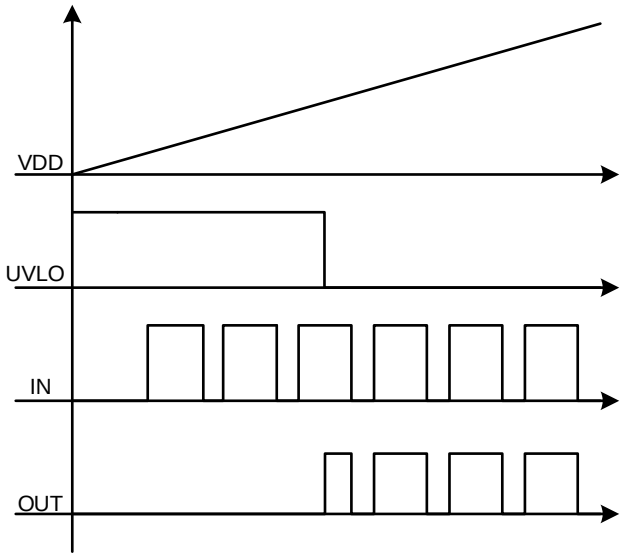


Figure 11. SCT52240 Output Vs VDD

Enable Function

SCT52240 provides independent enable pins ENA and ENB for external control of each channel operation. The enable pins are based on a TTL compatible input-threshold logic that is independent of the supply voltage and is effectively controlled with logic signals from 3.3-V and 5-V microcontrollers. When applying a voltage higher than the high threshold (typical 2.1V) the pin, the SCT52240 enables all functions and starts gate driver operation. Driver operation is disabled when ENx voltage falls below its lower threshold (typical 1V). The ENx pins are internally pulled up to VDD with 400k pullup resistors. Hence, the ENx pins are left floating or Not Connected (N/C) for standard operation, where the enable feature is not required.

Input Stage

The input of SCT52240 is compatible on TTL input-threshold logic that is independent of the VDD supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Wider hysteresis offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5V. SCT52240 also features tight control of the input pin threshold voltage that ensures stable operation across temperature. The very low input parasitic capacitance on the input pins increases switching speed and reduces the propagation delay.

Output Stage

The SCT52240 output stage features the pull up structure with P-type MOSFET PM1 and N-type MOSFET NM1 in parallel, as shown in Figure 12. PM1 provides the pull up capability when OUT approaches VDD and the NM1 holds off state, which guarantees the driver output is up to VDD rail. The measurable on-resistance R_{OH} in steady state is the conduction resistance of PM1. NM1 provides a narrow instant peak sourcing current up to 4A to eliminate the turn on time and delay. During the output turn on transition, the equivalent hybrid pull on transient resistance is $1.5R_{OL}$, which is much lower than the DC measured R_{OH}.

The N-type MOSFET NM2 composes the output stage pull down structure; the R_{OL} is the DC measurement and represents the pull down impedance. The output stage of SCT52240 provides rail-to-rail operation, and is able to supply 4A sourcing and 4A sinking peak current. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots. The outputs of the dual channel drivers are designed to withstand 500-mA reverse current without either damaging the device or logic malfunction.

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved

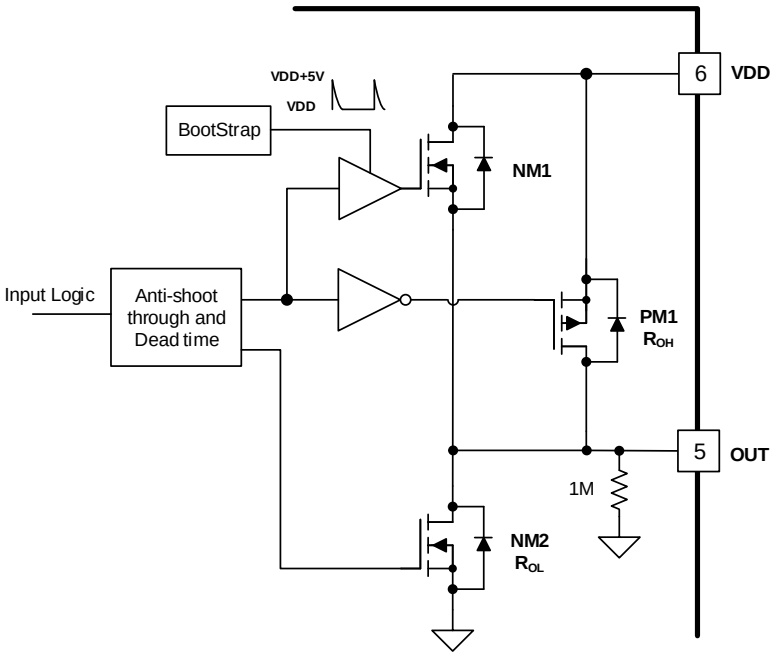


Figure 12. SCT52240 Output Stage

Stackable Output

The SCT52240 features 1ns (typical) delay matching between dual channels, which enables dual channel outputs be stackable when the driven power device required higher driving capability. For example, in a Boost Power Factor Correction converter, there are 2 power MOSFET in parallel to support higher power output capability. The two power MOSFET are preferred to be driven by a common gate control signal. By using SCT52240, the OUTA and OUTB can be connected together to provide the higher driving capability, so does the INA and INB. As a result, a single input signal controls the stacked output combination. To support the stackable output, each channel output stage artificially implements up to 5ns dead-time to avoid the possible shoot-through between two channels as

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved

Typical Application

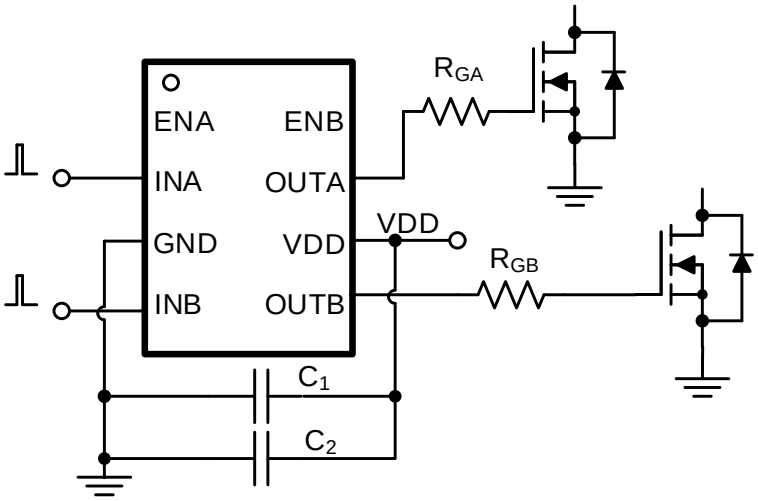


Figure 16. Dual Channel Driver Typical Application

Driver Power Dissipation

Generally, the power dissipated in the SCT52240 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52240 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of each channel in SCT52240 is:

(1)

Where

- V_{DD} is supply voltage
- C_{Load} is the output capacitance
- F_{SW} is the switching frequency

For the the switching load of power MOSFET, the power loss of each channel in the SCT52240 is shown in equation (2), where charging a capacitor is determined by using the equivalence $Q_g = C_{LOAD}V_{DD}$. The gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions.

(2)

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

If R_G applied between driver and gate of power device to slow down the power device transition, the power dissipation of the driver shows as below:

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved

– (——— ———) (3)

Where

- R_{OH} is the equivalent pull up resistance of SCT52240
- R_{OL} is the pull down resistance of SCT52240
- R_G is the gate resistance between driver output and gate of power device.

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved

Application Waveforms

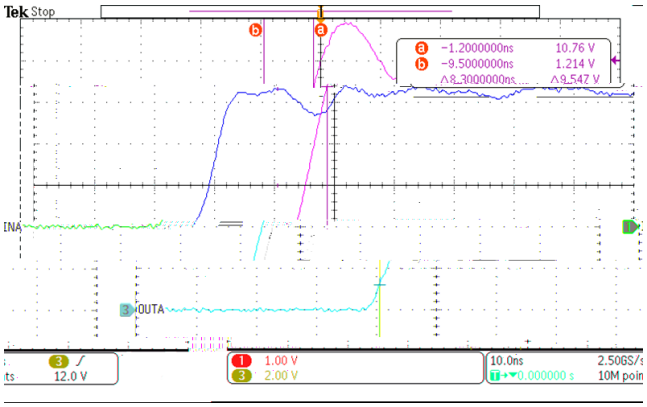


Figure 17. Driver Switching ON

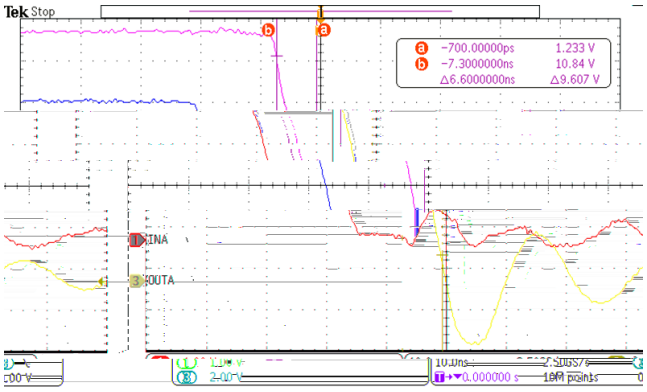


Figure 18. Driver Switching OFF

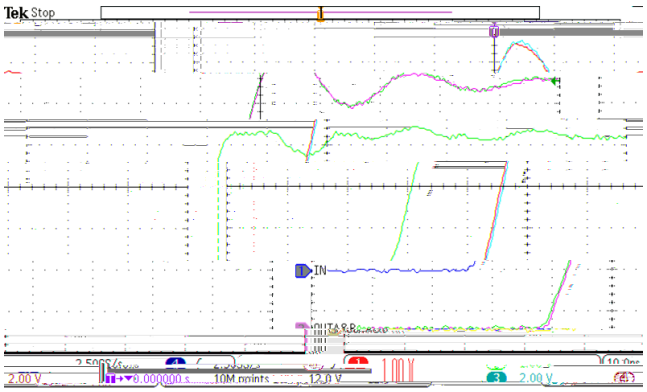


Figure 19. Delay Matching Rise

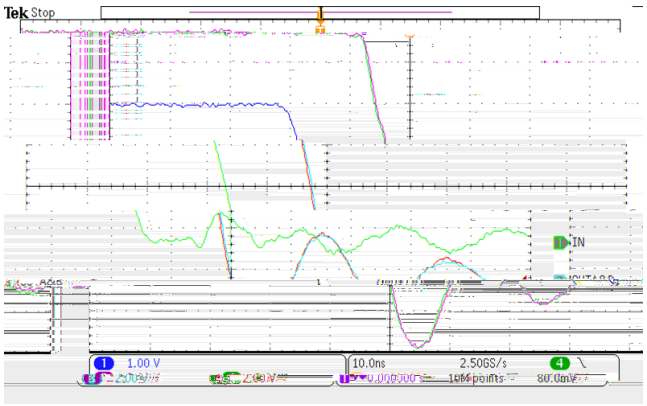


Figure 20. Delay Matching Fall

Figure 21. Stackable Output Rise

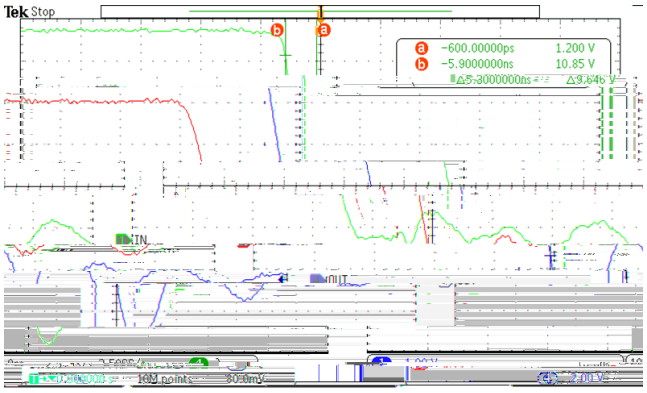


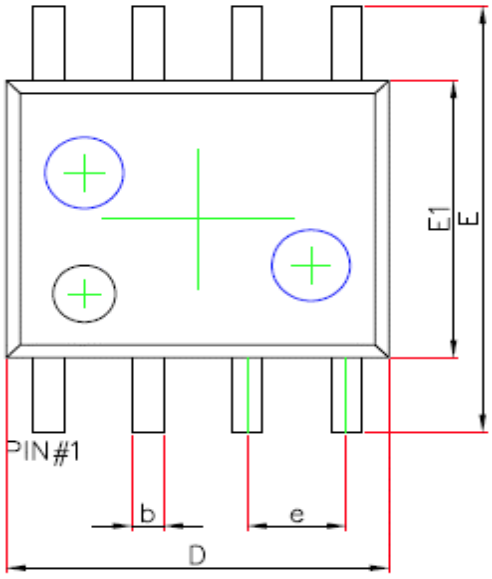
Figure 22. Stackable Output Fall

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved

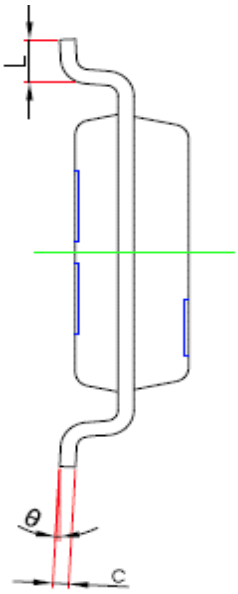
Layout Guideline

The SCT52240 provides the 4A output

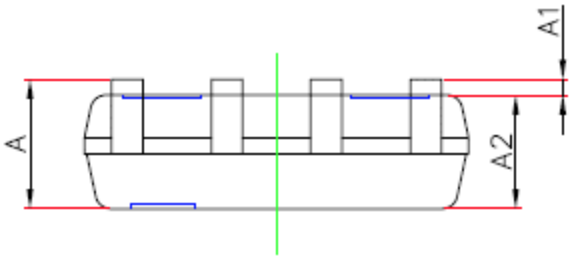
 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved



TOP VIEW



BOTTOM VIEW



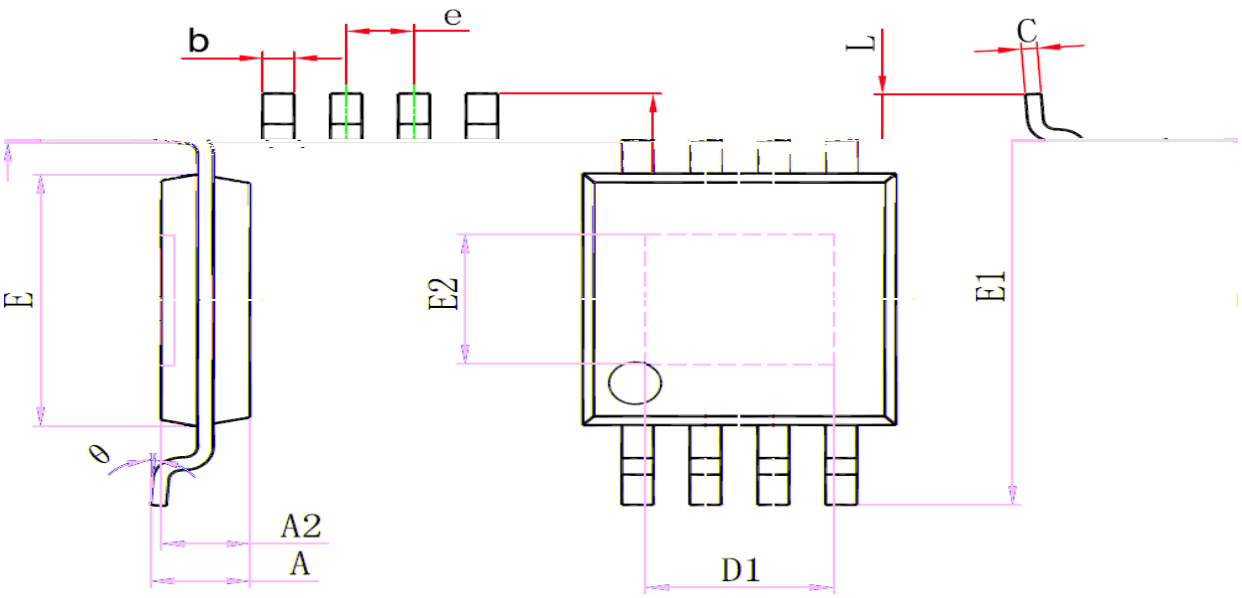
SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	1.45	---	1.75
A1	0.1	---	0.25
A2	1.35	---	1.55
b	0.33	---	0.51
c	0.17	---	0.25
D	4.7		5.1
E	5.8		6.2
E1	3.8		4.0
e	1.27BSC		
L	0.4		1.27
	0°		8°

NOTE:

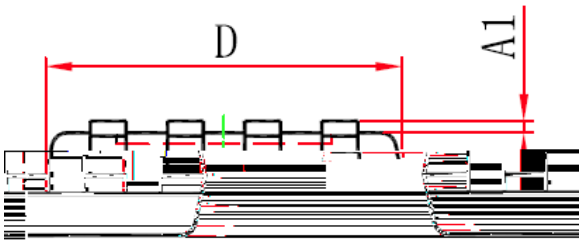
1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved



TOP VIEW

BOTTOM VIEW



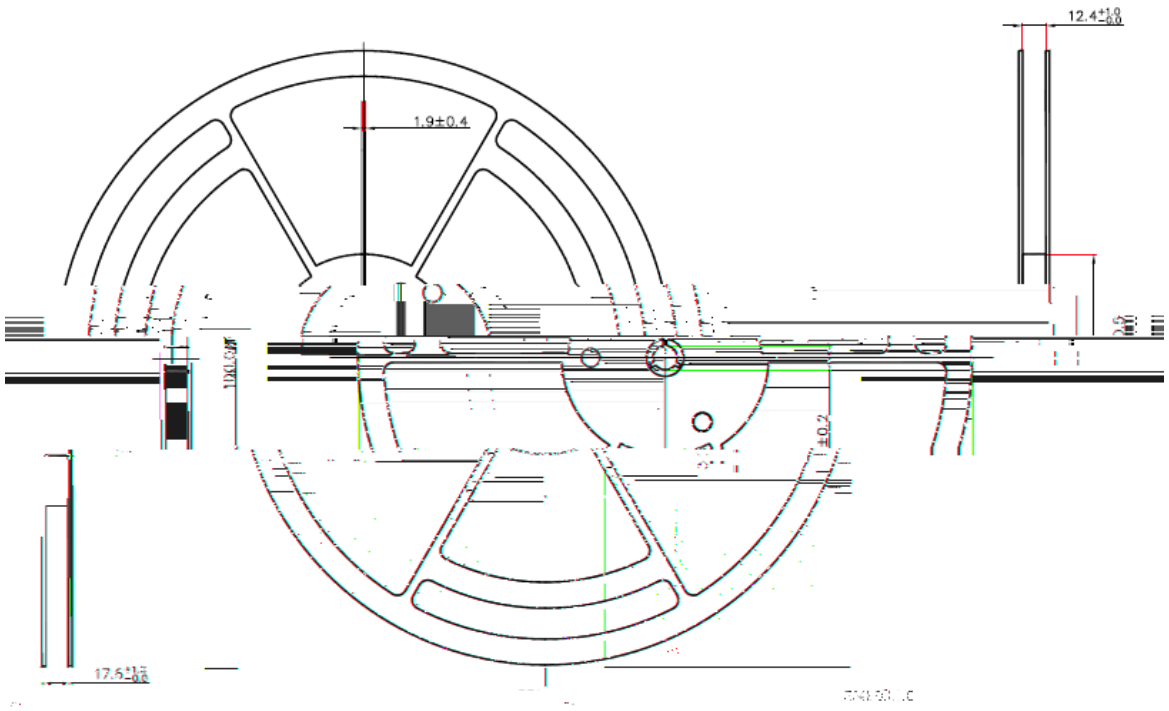
SIDE VIEW

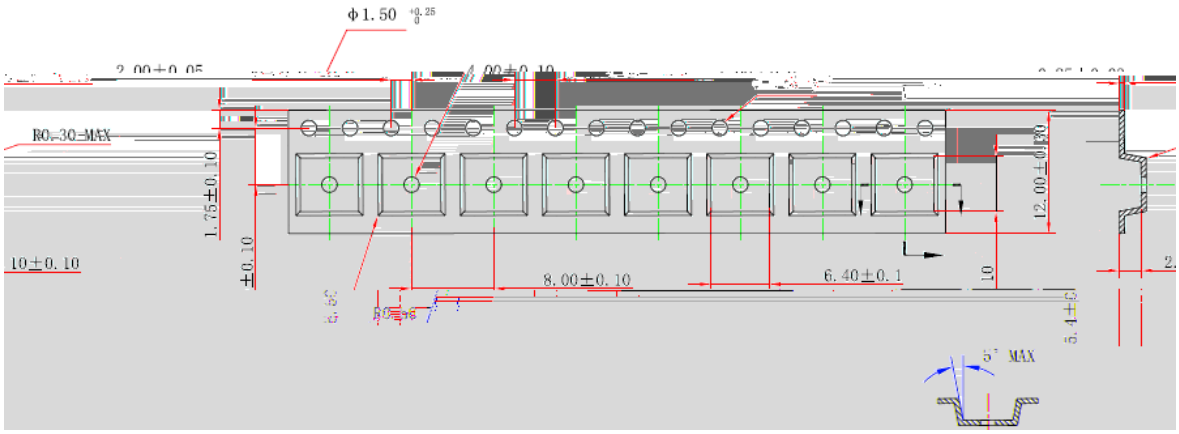
SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	0.82	---	1.1
A1	0.02	---	0.15
A2	0.75	---	0.95
b	0.25	---	0.38
c	0.09	---	0.23
D	2.9		3.1
D1	1.7		1.9
E	2.9		3.1
E1	4.75		5.05
E2	1.45		1.65
e	0.65BSC		
L	0.4		0.8
	0°		6°

NOTE:

7. Drawing proposed to be made a JEDEC package outline MO-220 variation.
8. Drawing not to scale.
9. All linear dimensions are in millimeters.
10. Thermal pad shall be soldered on the board.
11. Dimensions of exposed pad on bottom of package do not include mold flash.
12. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved

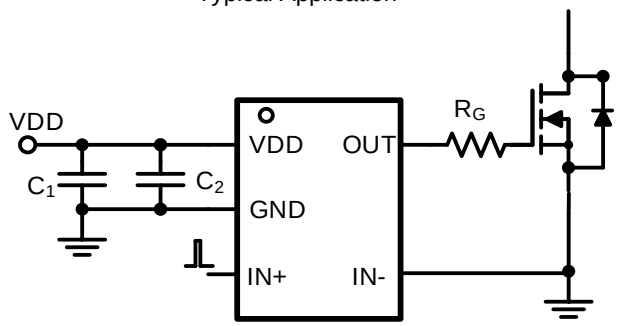




Feeding Direction

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved

Single Channel, Non-Inverting MOSFET Gate Drive
Typical Application



Typical Application Waveform

PART NUMBERS	DESCRIPTION

 © 2018 Silicon Content Technology Co., Ltd. All Rights Reserved