- Qualified for Automotive Applications
- Wide Input Voltage Range: 3.2V-50V
- Low Shutdown Current 3.7uA
- Low Quiescent operating Current: 450uA
- Adjustable Switching Frequency: 100KHz to 2.2MHz
- Integrated Frequency Dithering for EMI Mitigation
- External Frequency Synchronic
- External Compensation
- Supports additional Slope Compensation
- 22ms Internal Soft-start Time
- Integrated Protection Feature
  - Constant Peak-Current Protection Threshold Over Input Voltage
  - Output Overvoltage Protection
  - Adjust Under-Voltage Lockout
  - Optional Hiccup Over Load Protection
  - Thermal Shutdown Protection:165°C
- MSOP-8L(3mm*3mm) Package

- Muti-output Flyback
- LED Bias Supply
- Portable Speaker Supply
- Battery Powered Boost/Flyback/SEPIC application

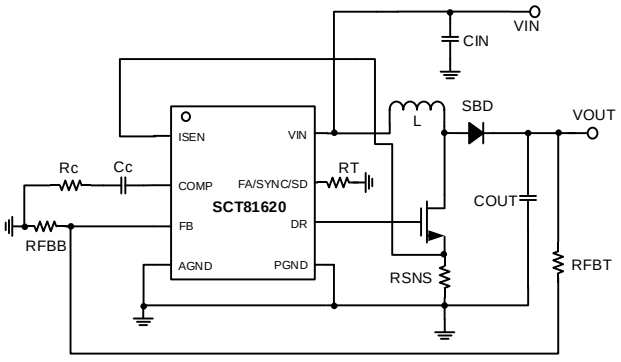
The SCT81620 device is a wide input, non-synchronous boost controller. The Device can be used in Boost, SEPIC and Flyback converters and topologies.

The switching frequency of the SCT81620 device can be adjusted to any value between 100kHz and 2.2MHz by using a single external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response in addition to cycle-by-cycle current limiting. Current limit is adjustable through an external resistor.

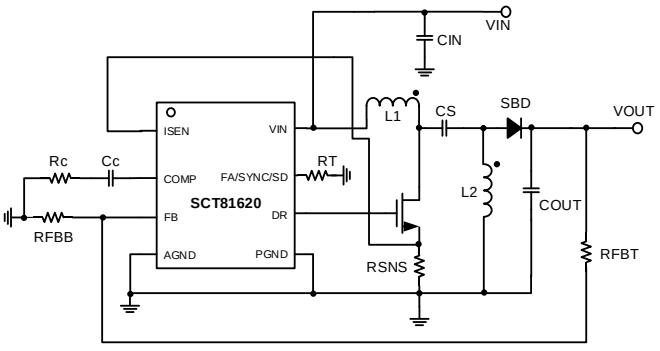
The SCT81620 is an Electromagnetic Interference (EMI) friendly controller with implementing optimized design for EMI reduction. The SCT81620 features Frequency Spread Spectrum (FSS) with ±6% jittering span of the switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The SCT81620 device has built-in protection features such as thermal shutdown, short-circuit protection and overvoltage protection. Power-saving shutdown mode reduces the total supply current to 3.7 µA. Integrated current slope compensation simplifies the design and, if needed for specific applications, can be increased using a single resistor.

The device is available in a MSOP-8L(3mm*3mm) Package.



BOOST



SEPIC

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Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.2	50	V
V_{CC}	VCC voltage range	3.2	6.1	V
T_J	Operating junction temperature	-40	125	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins	-1	+1	kV

PARAMETER	THERMAL METRIC	MSOP-8	UNIT
R	Junction to ambient thermal resistance(1)	132.8	°C/W
R (top)	Junction to case (top) thermal resistance(1)	64.1	°C/W
R B	Junction to board thermal resistance(1)	83.8	°C/W

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT81620 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT81620. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{ON_MIN}	Minimum on-time	Fsw=400kHz		250		ns
Protection						
V_{OVTH}(3)	FB overvoltage threshold	FB rising	25	85	135	mV
		Hysteresis	30	80	130	mV
T_{SD}(1)	Thermal shutdown threshold	T_J rising		165		°C
	Hysteresis			25		°C

(1) Guaranteed by design and bench, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) The overvoltage protection is specified with respect to the feedback voltage. This is because the overvoltage protection tracks the feedback voltage. The overvoltage threshold can be calculated by adding the feedback voltage (V_{FB}) to the overvoltage protection specification.

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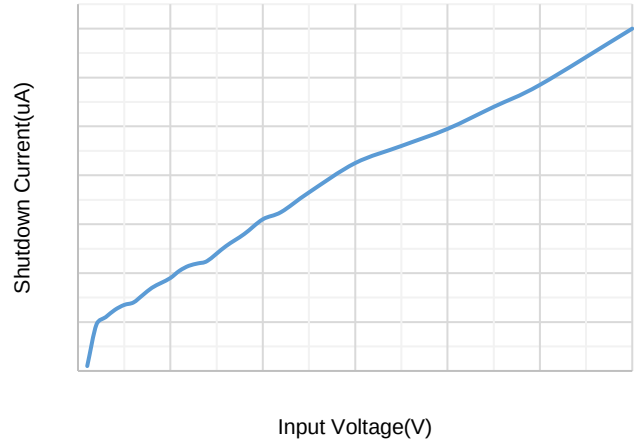

Figure 1. ISD vs Input Voltage

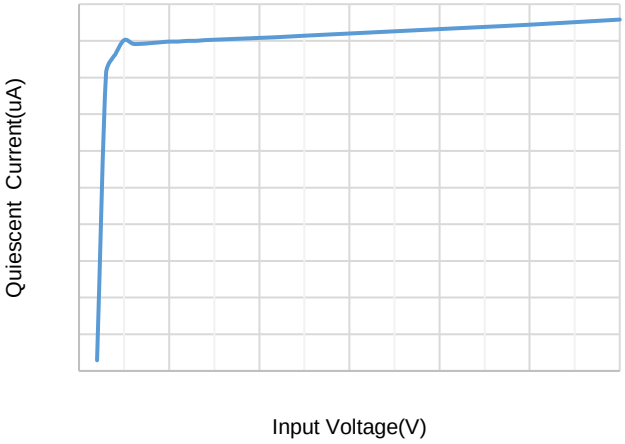

Figure 2. IQ vs Input Voltage

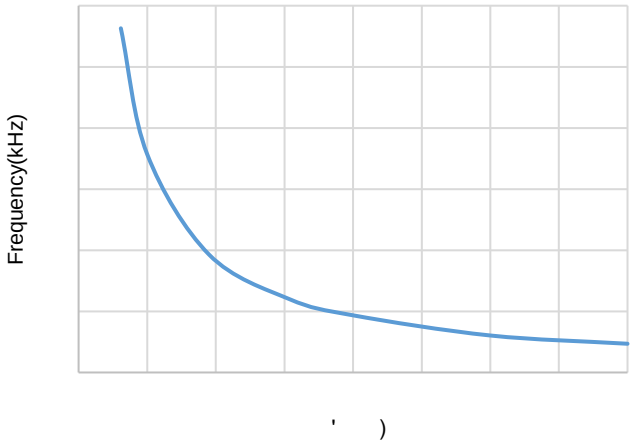

Figure 3. Switching Frequency vs RT

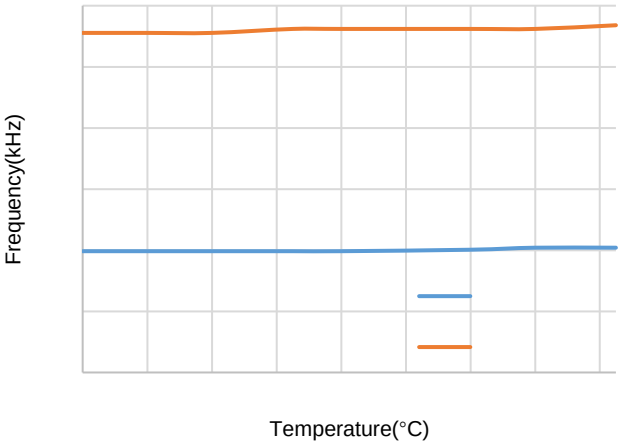

Figure 4. Switching Frequency vs Temperature

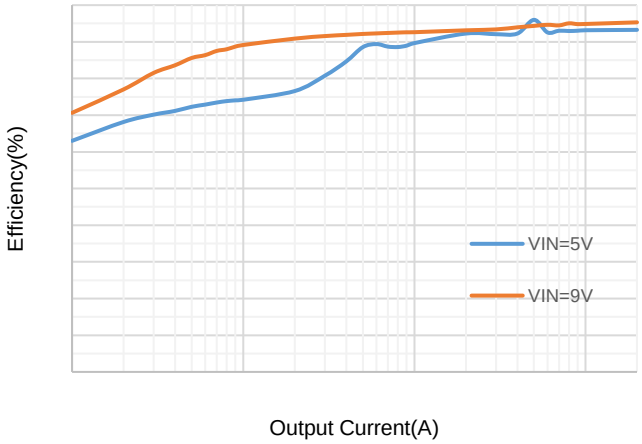

Figure 5. Efficiency vs Load Current, Boost, VOUT=12V

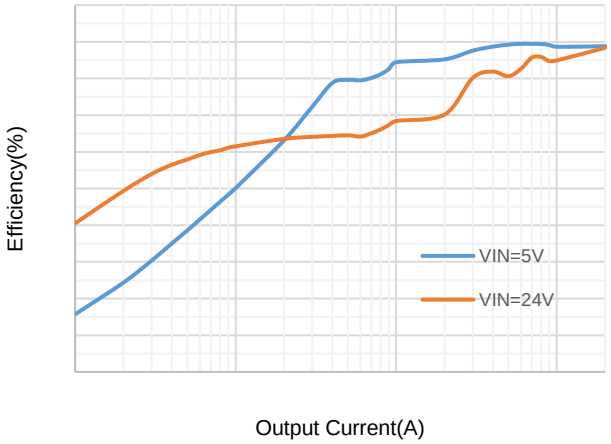

Figure 6. Efficiency vs Load Current, Sepic, VOUT=12V

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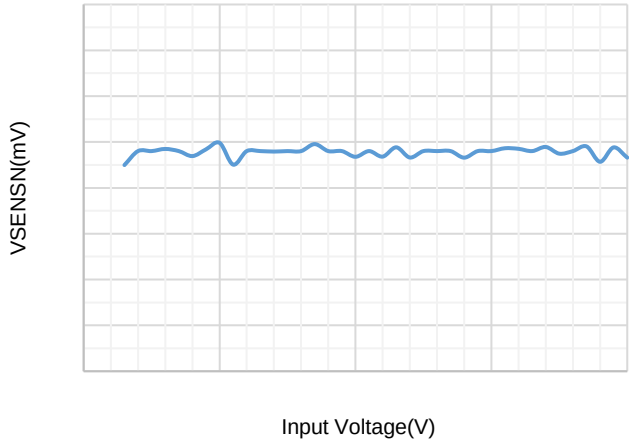

Figure 7. VSENSN vs Input Voltage

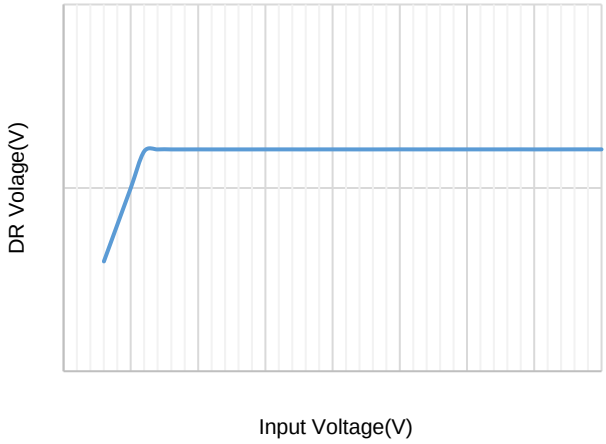

Figure 8. DR Volage vs Input Voltage

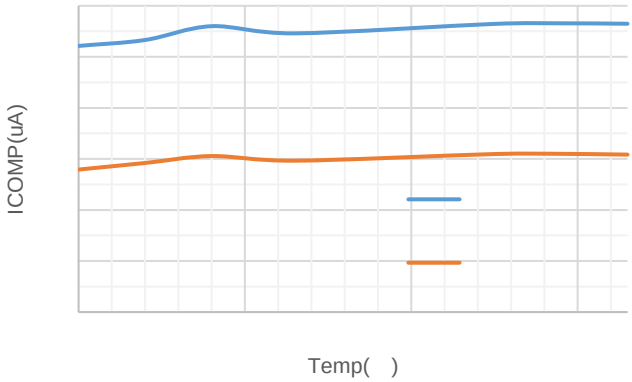

Figure 9. COMP Current vs Temperature

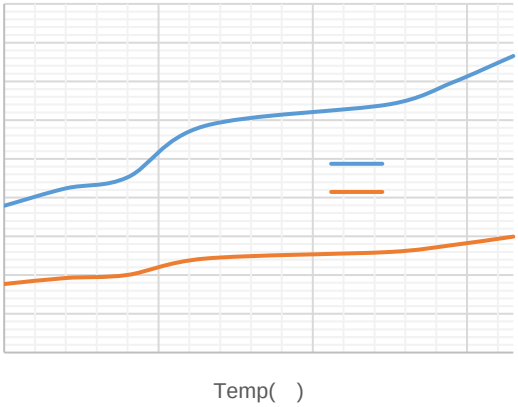

Figure 10. DR Resistance vs Temperature

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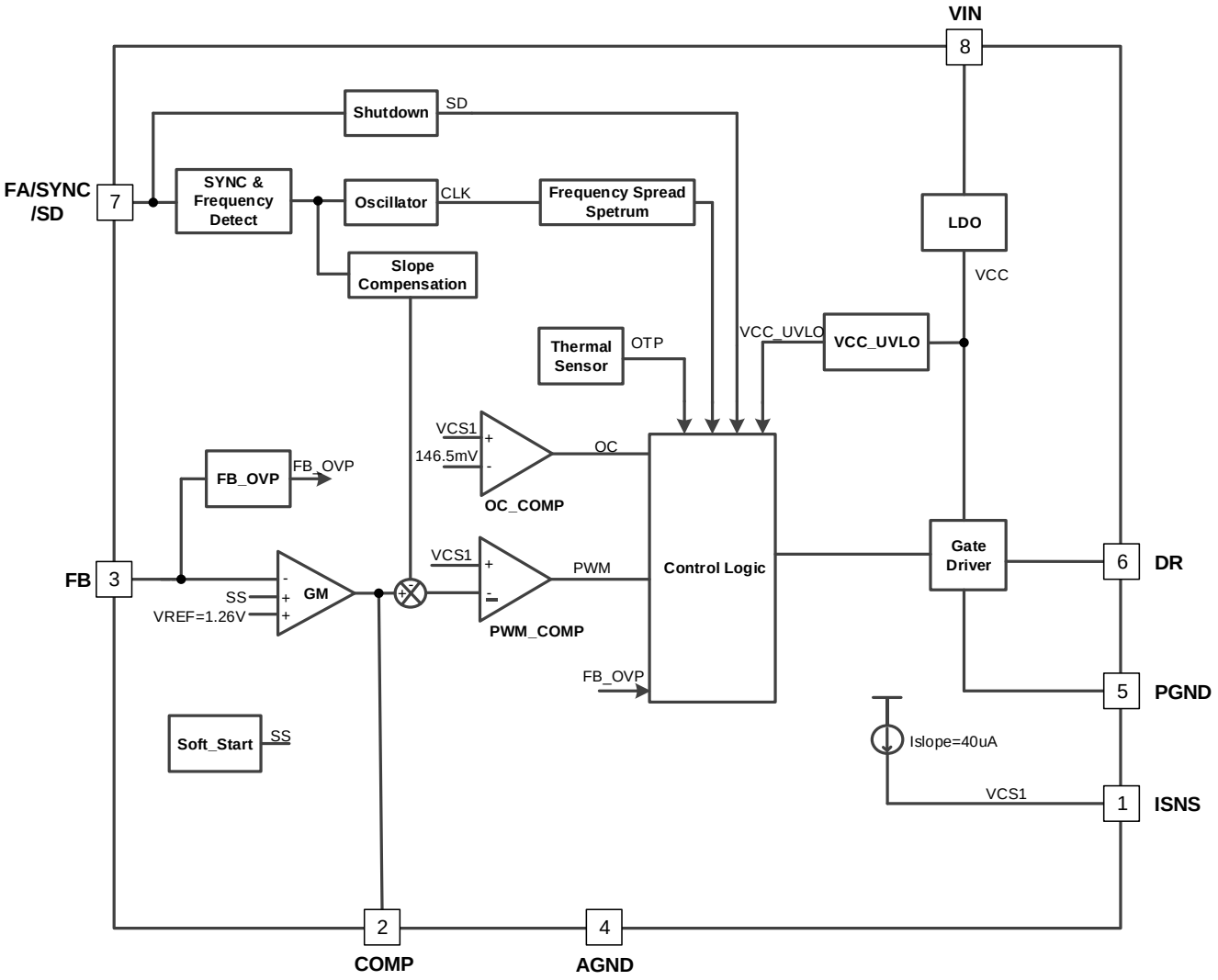

Figure 11. Functional Block Diagram

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Overview

Overvoltage Protection

Slope Compensation Ramp

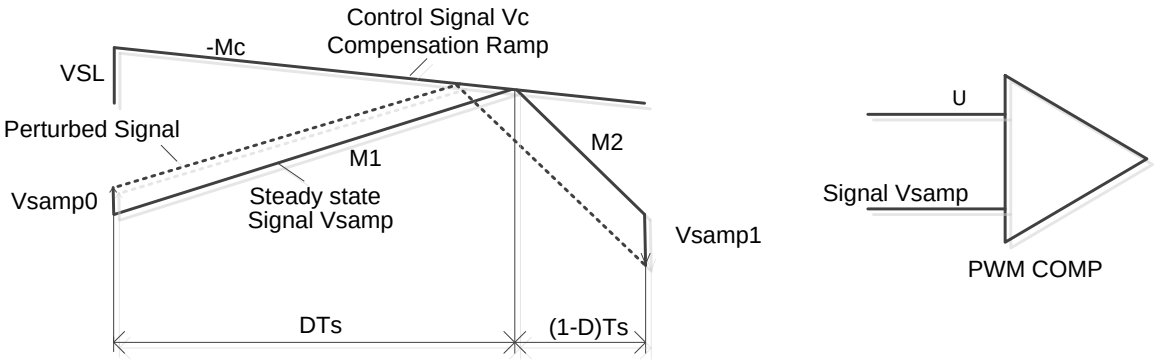

Figure12. Sub-Harmonic Oscillation for D>0.5 and Compensation Ramp to Avoid Sub-Harmonic Oscillation

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$$V_{samp} = I_L * R_{SEN} \quad (1)$$

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$$M_1 = M_{on} * R_{SEN} \quad (2)$$

$$-M_2 = -M_{off} * R_{SEN} \quad (3)$$

& * %

$$M_1 = M_{on} * R_{SEN} = Vin * R_{SEN} / L \quad (4)$$

$$M_2 = M_{off} * R_{SEN} = (Vout - Vin) * R_{SEN} / L \quad (5)$$

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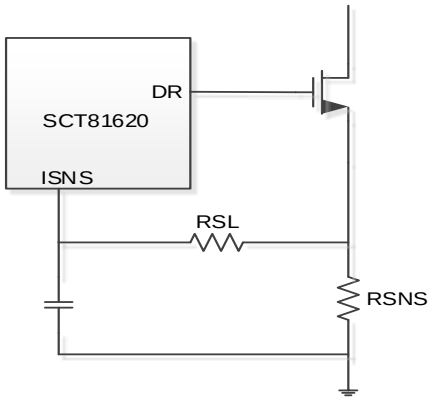

Figure13 .External RSL to increase slope compensation

Adjustable Peak Current Limit

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$$I_{PEAK_CL} = \frac{V_{SENSE} - 40uA \times R_{SL} \times D}{R_{SNS}} \quad (11)$$

Where

- V_{SENSE} is ISEN pin limiting voltage (Typ.=146.5mV)
- $I_{PEAK-CL}$ is the inductor peak current limit
- R_{SL} is Slope compensation resistor
- D is Duty cycle
- R_{SNS} is the Inductance peak current detection resistance

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Output Voltage

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$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (12)$$

where:

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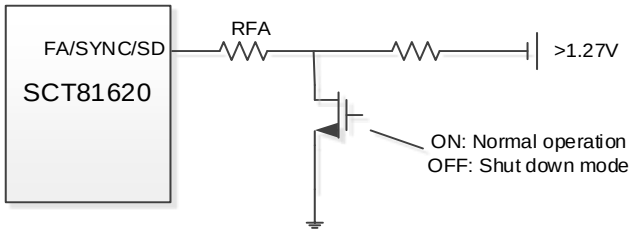

Figure17. Shutdown operation in Frequency Adjust Mode

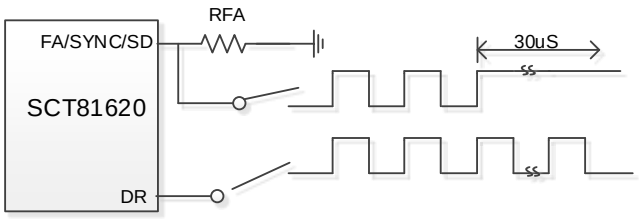

Figure18. Shutdown operation in Frequency Synchronization Mode

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Typical Application (Boost)

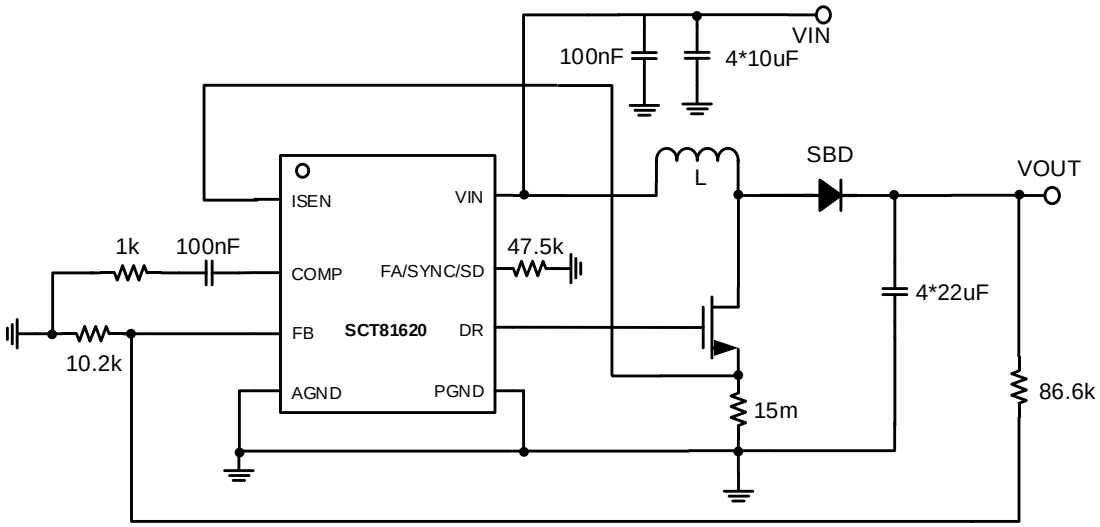

Figure 19. Application Schematic, 3V to 11V, 2A Boost Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal 3V to 11V
Output Voltage	12V
Maximum Output Current	3A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

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Where

I_G is the gate drive current.

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Output Diode Selection

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$$I_{D(PEAK)} = \frac{I_{OUT}}{(1-D)} + \Delta I_L \quad (24)$$

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Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

Figure 20. Power up(Iload=2A)

Figure 21. Power down(Iload=2A)

Figure 22. Over current protection (Iload=5A)

Figure 23. Over

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Typical Application (Sepic)

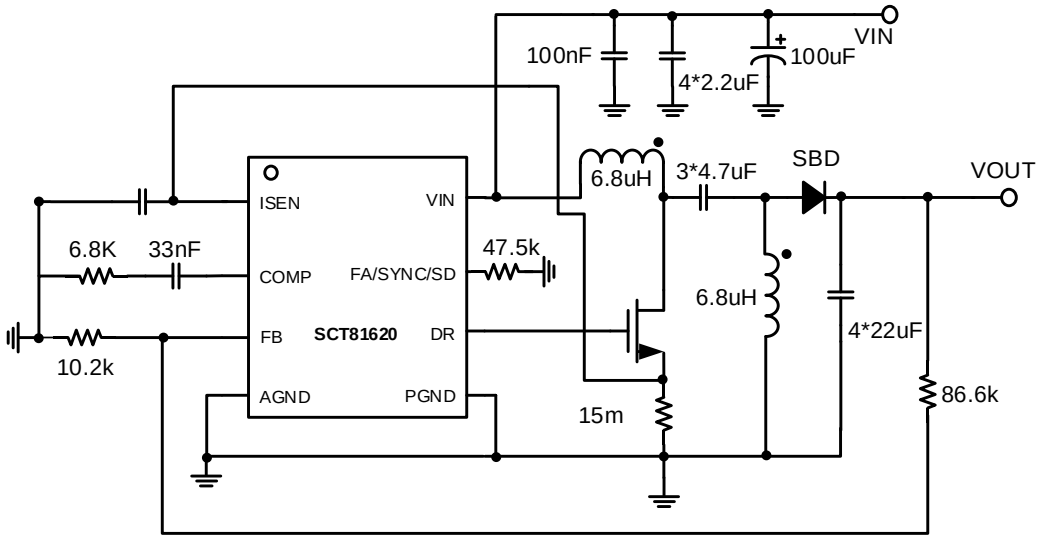

Figure 26. Application Schematic, 5V to 50V, 2A Sepic Regulator at 400kHz

Design Parameters

Design Parameters

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Inductor Selection (Sepic)

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$$\Delta I_{L1} = I_{IN} \times 40\% = I_O \times \frac{V_O}{V_{IN_MIN}} \times 40\% \quad (25)$$

$$\Delta I_{L2} = I_O \times 40\% = I_O \times 40\% \quad (26)$$

* * * * & ' '

$$L_1 = L_2 = L = \frac{V_{IN_MIN}}{\Delta I_L \times f_{SW}} \times D_{MAX} \quad (27)$$

&

- f_{SW} is the switching frequency.

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$$I_{L1_PEAK} = I_{IN} + \frac{\Delta I_L}{2} = I_O \times \frac{V_O}{V_{IN_MIN}} \times (1 + \frac{40\%}{2}) \quad (28)$$

$$I_{L2_PEAK} = I_O + \frac{\Delta I_L}{2} = I_O \times (1 + \frac{40\%}{2}) \quad (29)$$

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$$L_1 = L_2 = \frac{L}{2} = \frac{V_{IN_MIN}}{2 \times \Delta I_L \times f_{SW}} \times D_{MAX} \quad (30)$$

Power MOSFET Selection

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$$V_{SW_PEAK} = V_{IN} + V_O + V_D \quad (31)$$

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$$I_{Q_PEAK} = I_{L1_PEAK} + I_{L2_PEAK} \quad (32)$$

& & %& & ' * *

$$I_{Q_RMS} = I_O \times \sqrt{\frac{\left(V_O + V_{IN_MIN} + V_D\right) \times \left(V_O + V_D\right)}{V_{IN_MIN}^2}} \quad (33)$$

& ' ' ' '

$$P_{DIS} = I_{Q_RMS}^2 \times R_{DS_ON} \times D_{MAX} + \left(V_O + V_{IN_MIN}\right) \times I_{Q_PEAK} \times \frac{Q_g \times f_{SW}}{I_G} \quad (34)$$

&

- *I_G is the gate drive current.*

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Output Diode Selection

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$$V_{D_PEAK} = V_{IN_MAX} + V_{O_MAX} \quad (35)$$

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Coupling Capacitor Selection

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$$\Delta V_{CS} = \frac{I_O \times D_{MAX}}{C_S \times f_{SW}} \quad (36)$$

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' % & '

& * % ' ' %

$$I_{CS_RMS} = I_O \times \sqrt{\frac{V_O + V_D}{V_{IN_MIN}}} \quad (37)$$

& ' * %

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$$I_{COUT_RMS} = I_O \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}} \quad (41)$$

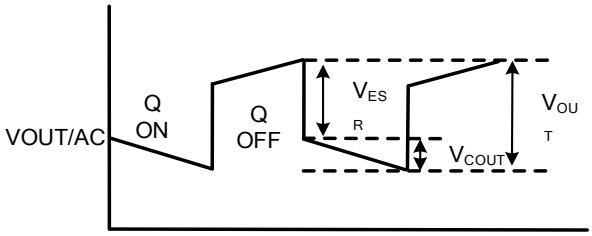

Figure 27. Output Voltage Ripple

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Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

Figure 28. Power up(Iload=2A)

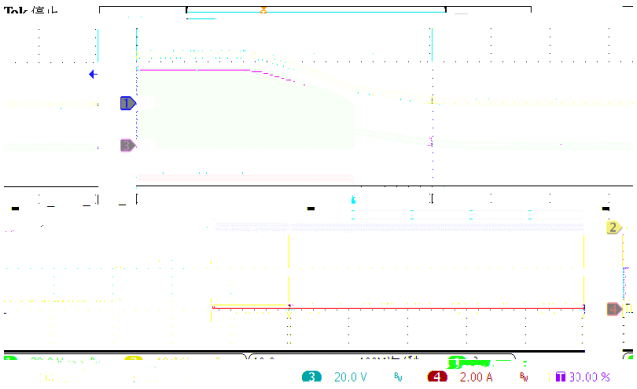

Figure 29. Power down(Iload=2A)

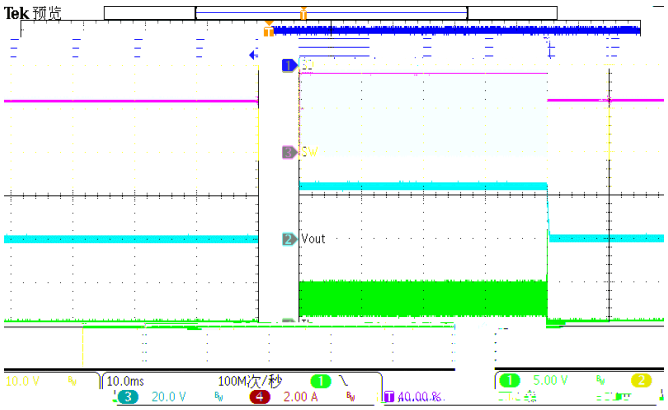

Figure 30. Shutdown remove

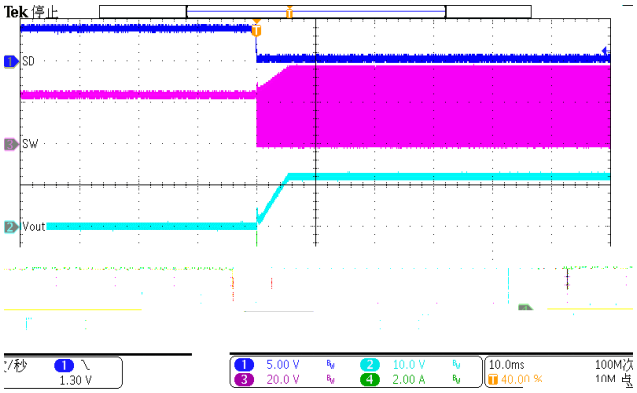

Figure 31. Shutdown remove

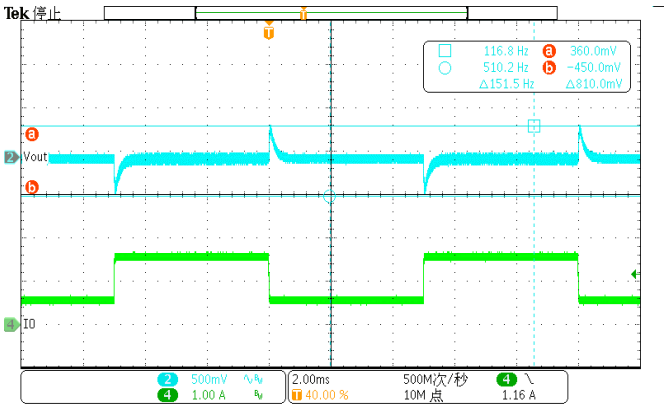

Figure 32. LoadTrans (Iload=0.5A-1.5A)

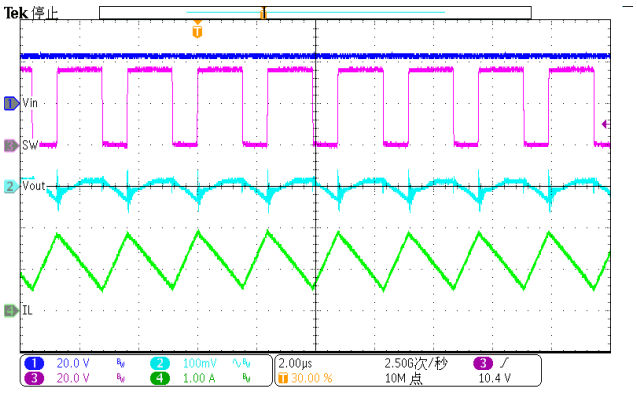

Figure 33. steady-state (Iload=2A)

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Layout Guideline

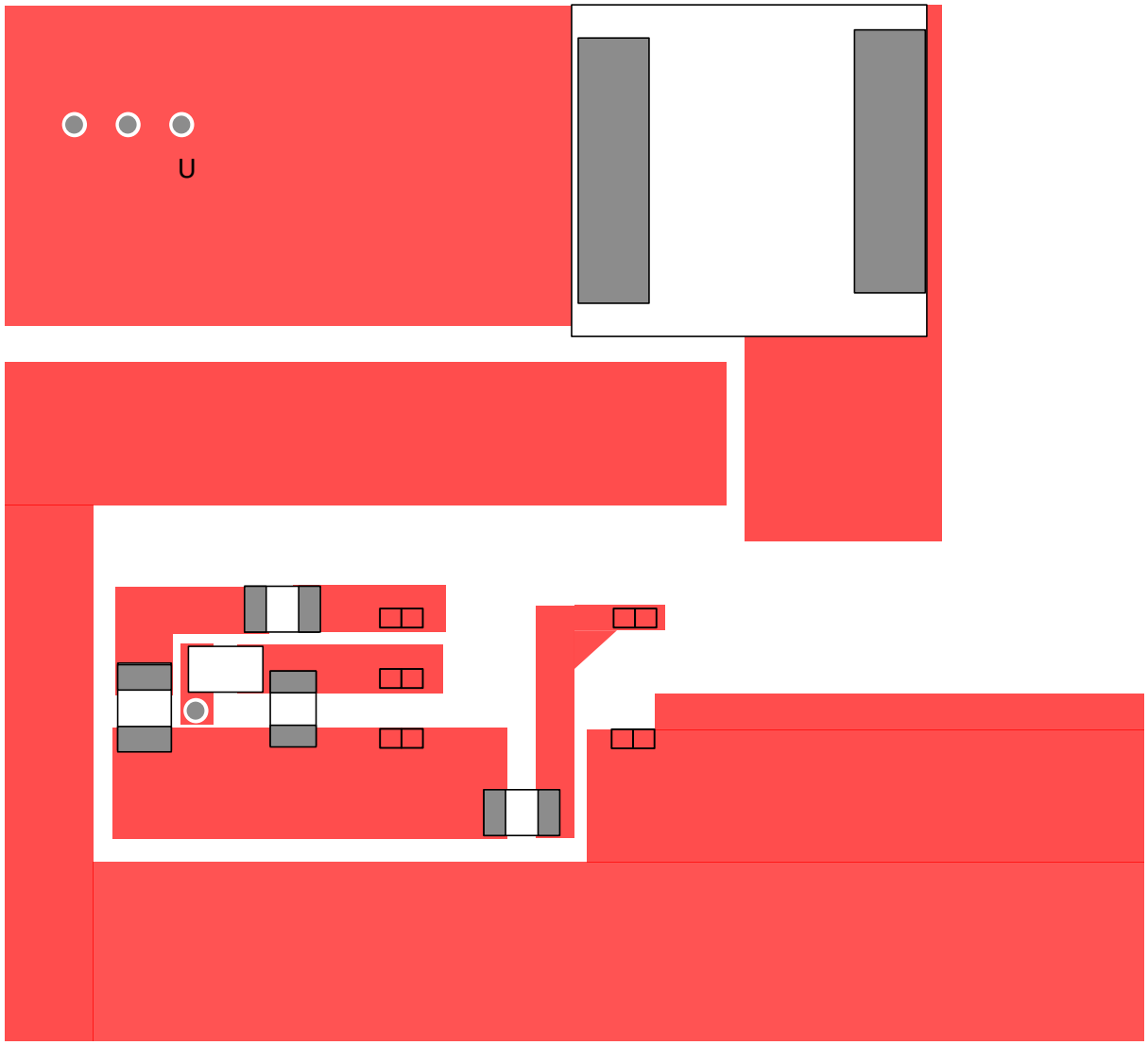

Figure 34. BOOST PCB Layout

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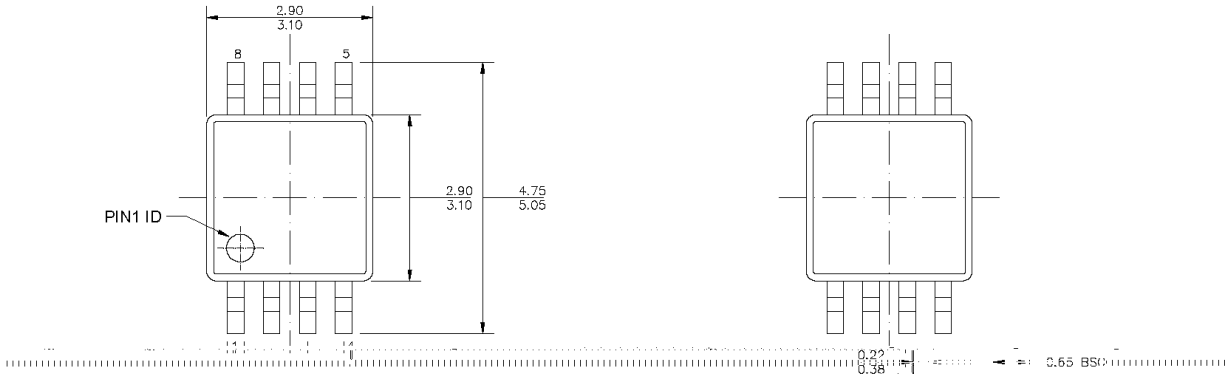
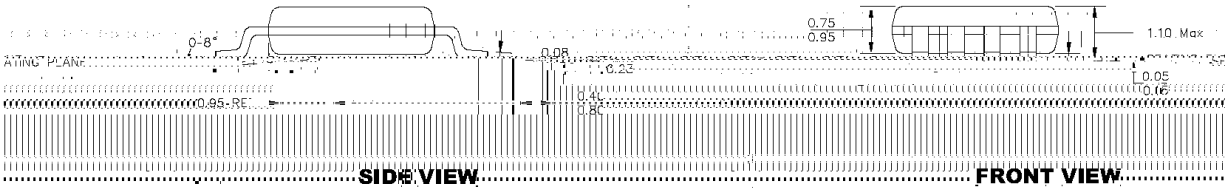


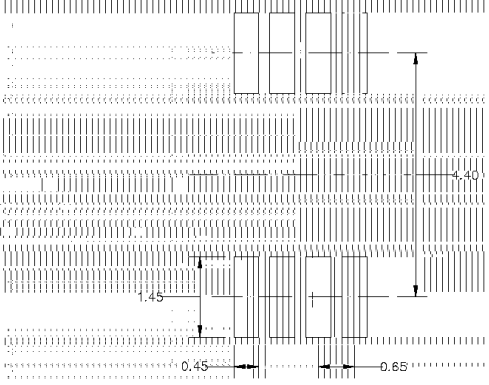
BOTTOM VIEW **TOP VIEW**



SIDE VIEW **FRONT VIEW**

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) DRAWING MEETS JEDEC MO-187, VARIATION BA.
4) DRAWING IS NOT TO SCALE.



RN **RECOMMENDED LAND PATTE**

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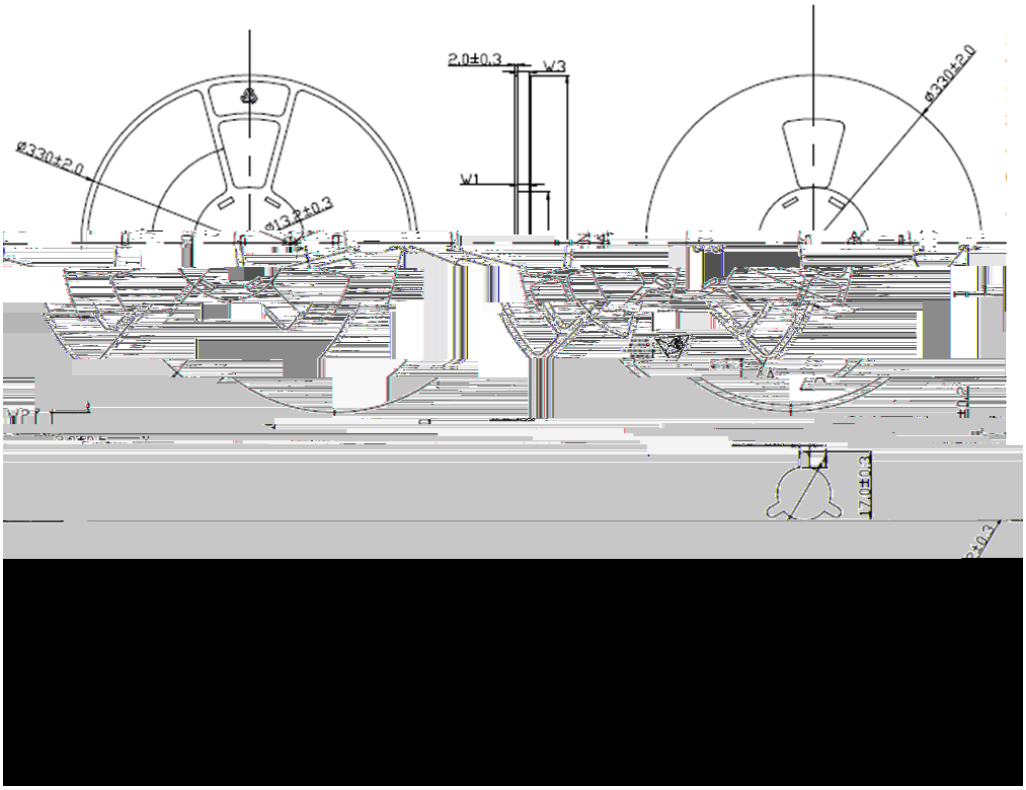

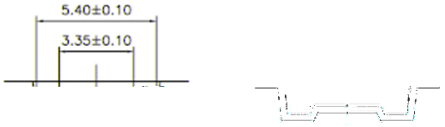

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