

5.5V-100V Vin, 4A Peak Current Limit, High Efficiency Asynchronous Step-down DCDC Converter

FEATURES

- *%%
- *
- 1 3 3
- 1 3
- %
- 1 3
-
-
-
- 3 3

REVISION HISTORY

*					
*	4	3	4		1
*		1 2			

DEVICE ORDER INFORMATION

3 1 &			1 &	(	(	

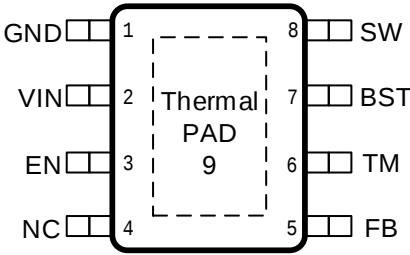
ABSOLUTE MAXIMUM RATINGS

2		&	
2		&	
2		& & %	
		%	3
	& %	%	3

(1) 1 3

(2)

PIN CONFIGURATION



	(	3
	)	32 4

RECOMMENDED OPERATING CONDITIONS

		%%		
			%	3

ESD RATINGS

4	2 2 1 4 3			
	3 4 34 1 4 3			
(1) 4 3	%% % 2		4	
(2) 4 3	% % 34		4	

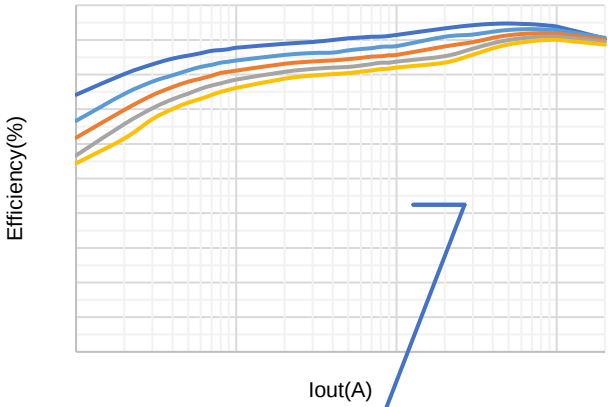
THERMAL INFORMATION

1			3
3		%(	
3 1 3	1 3	1 3	
32 3 1 &	3 1 & 3	32 32	
	1 3		

ELECTRICAL CHARACTERISTICS

- (	-	3	%3	%3	
				%%	

TYPICAL CHARACTERISTICS



The schematic diagram illustrates the control logic for a buck converter. Key components and connections include:

- EN Pin:** The Enable pin is connected to a pull-up resistor (0.3uA) and a diode. It is also connected to a 1.25V reference voltage and a 2.1uA current source. The EN pin is connected to the EN LOGIC VIN UVLO Reference block.
- EN LOGIC VIN UVLO Reference:** This block provides a reference voltage (VREF) and a VCC signal to the EN pin.
- Thermal Shutdown:** A block that monitors the temperature and provides a shutdown signal to the EN pin.
- Feedback Loop:** The feedback (FB) pin is connected to a voltage divider (1.2V) and a 0V pin. The 0V pin is connected to the FB pin through a 120%VREF resistor. The FB pin is connected to the Control Logic block.
- Control Logic:** A central block that receives inputs from the FB pin, EN pin, and various protection blocks. It outputs the SW (switch) signal to the BST (bootstrap) pin.
- Protection Features:**
 - Boot UVLO:** A block that monitors the bootstrap voltage and provides a UVLO signal to the Control Logic.
 - SW Pin:** The switch pin is connected to the SW signal and the BST pin.
 - BST Pin:** The bootstrap pin is connected to the BST signal and the SW pin.
 - VCC Pin:** The VCC pin is connected to the VCC signal and the SW pin.
 - GND Pin:** The GND pin is connected to the GND signal and the SW pin.

OPERATION

3	1	&	%%	1	4343	%
---	---	---	----	---	------	---

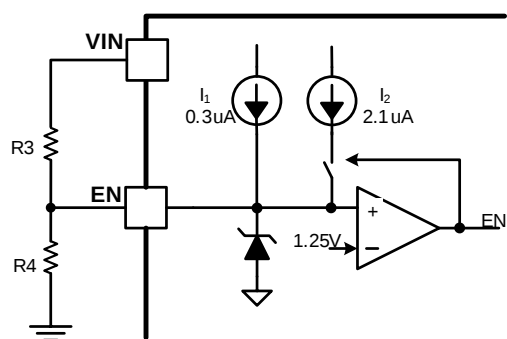
3 1 &

3 1 & %

3 1 &

3 1 & 3

3 1 & %& 1)



1
%

3 1 &

±

2

- 2
- 2 2

2

2

3 1 &

1

2

) %

%

2

3 1 &

3 1 &

3

2

3 1 &

2

%

2

2

3 1 &

& 3
3

(

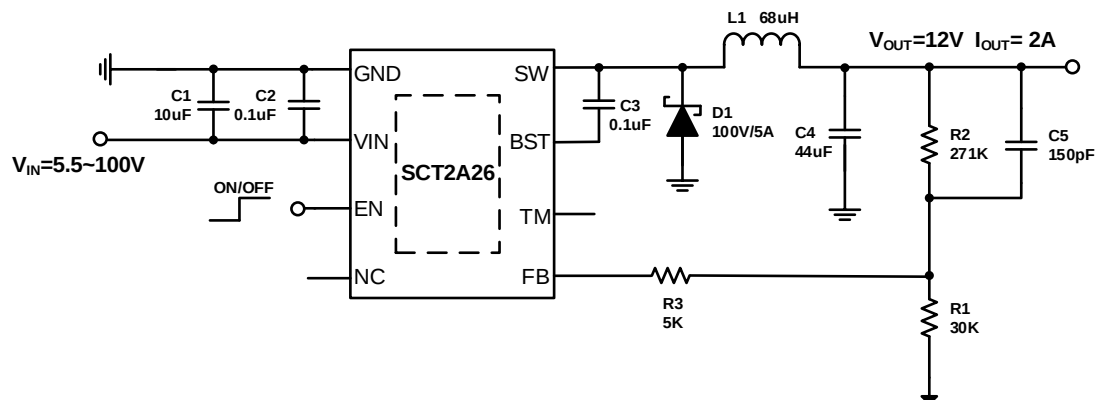
3

3

1

* 3 1 &

APPLICATION INFORMATION



-
- -

%

%

%1

1

%

13

3

4343

4343

%

43

&

4

1

-

*

43

%

%

%

1

1

%

2

1

&

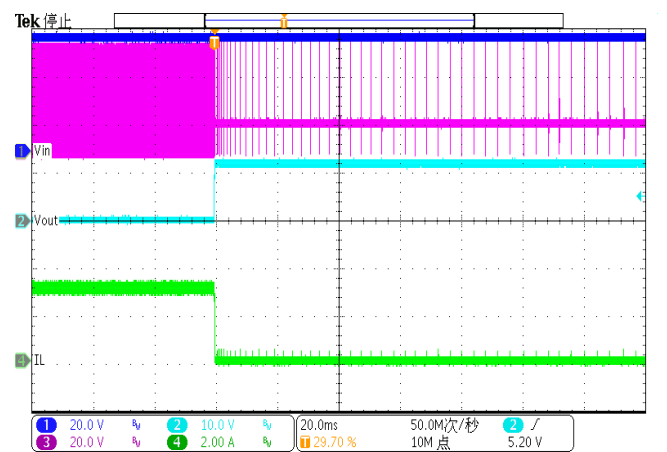
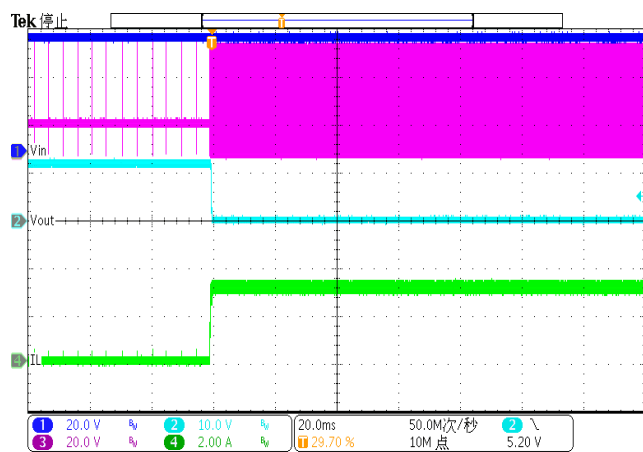
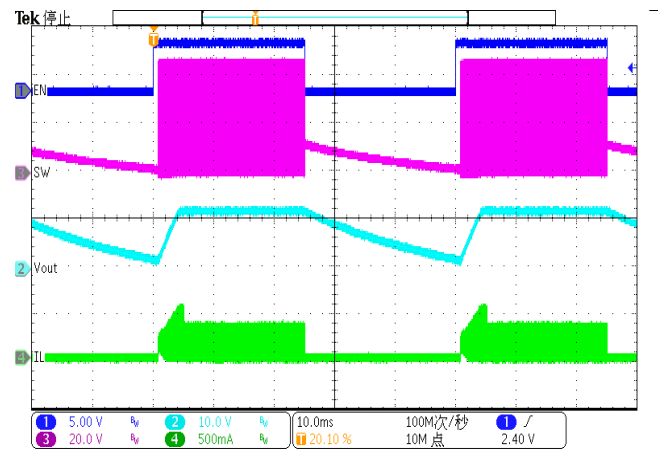
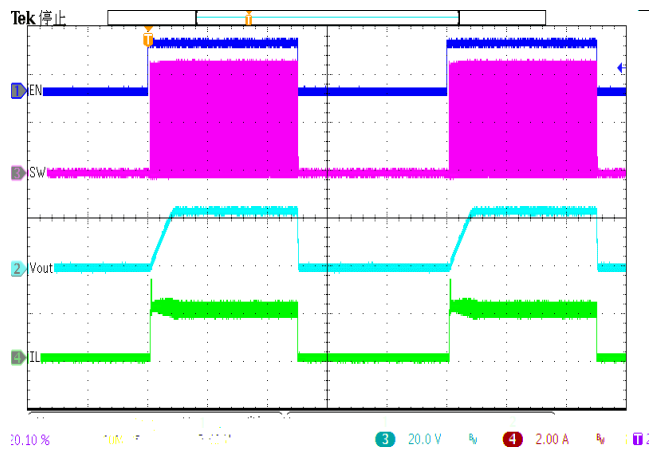
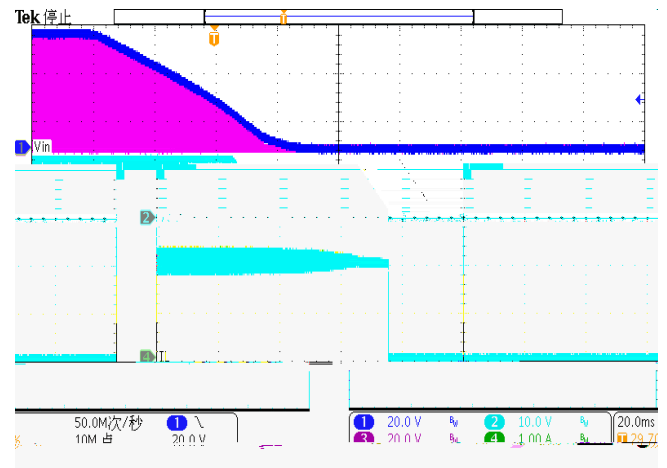
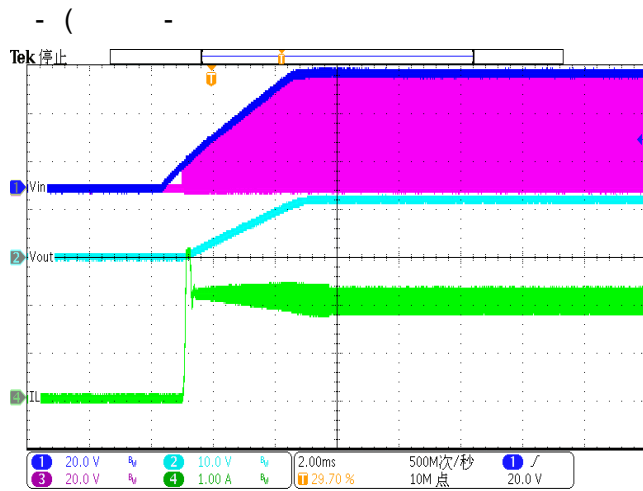
&

3

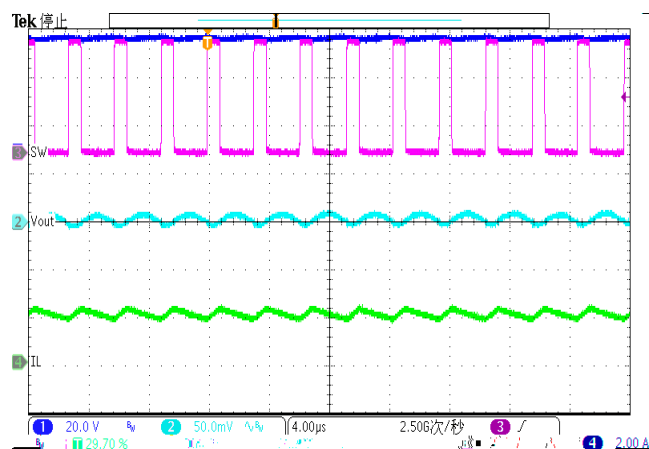
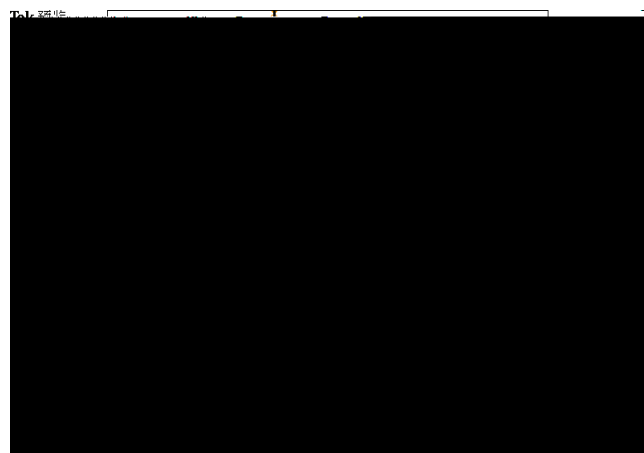
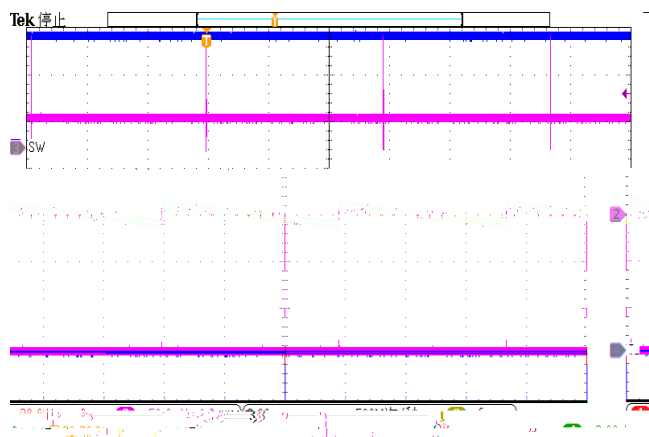
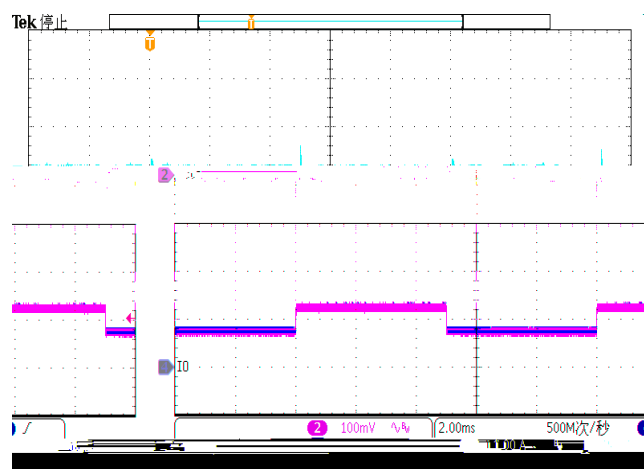
4

43

3



- (-



& 3 3 1

* 3 1 &

PACKAGE INFORMATION

() %

4

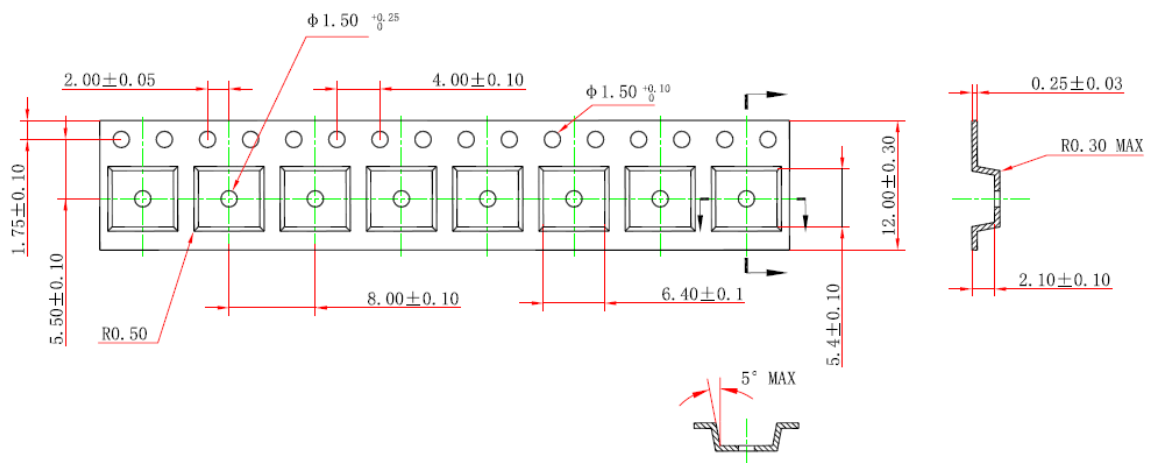
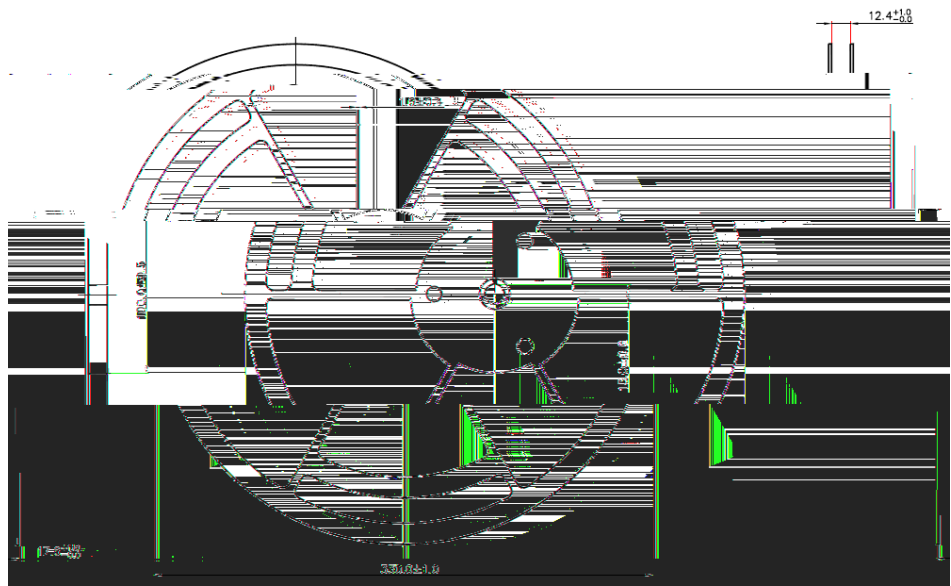
	4		4	
1			%	&
1				
1	%	%%	%	&
		%		
		%		
4		%	(%	
4	%	%		(
	(		%	%
	%(	&	(	
	&	&	(%	)
	2 3		% 2 3	
			&	%
θ		(		(

1. 4

4

3

TAPE AND REEL INFORMATION



3

3

3

(

3

3

1

* 3 1 &