3V-40V Vin, 150mA, 2.5uA I_Q, Low-Dropout Regulator

Wide Input Range: 3V-40V
With up to 45V Transient Input Voltage
Maximum Output Current: 150mA
Output Voltage:
- 3.3V and 5V (Fixed Output)
- Other Output Voltage Options (Need contact SCT sales)

Output Voltage Accuracy:
- T_J= 25 : 1%
- T_J= -40 ~ 125 : 2%

Low Quiescent Current: 2.5uA
Low Dropout Voltage
- 204mV at 50mA load current
- 643mV at 150mA load current

Support Output Capacitors Range:
- 3.3uF~220uF
- Low-ESR: 0.001Ω~ 5 Ω

660us Internal Soft-start Time
Integrated Short-Circuit Protection with OCFB (Over Current Fold-back) Feature
Over-Temperature Protection
Available Package:
SOT23-5L / SOT23-3L

Handheld Devices with Battery Power Supply
POS and Power Tools
Meters and Smoke Detector
Industrial Control

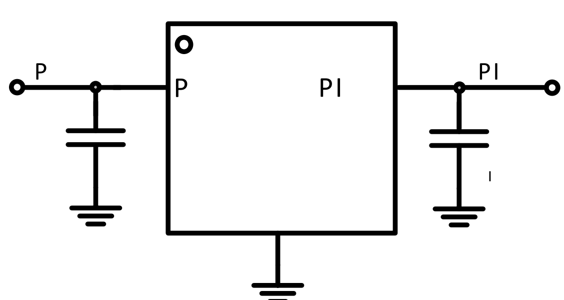
The SCT71401 series products is a low-dropout linear regulator designed to operate with a wide input-voltage range from 3 V to 40 V (45V transient input voltage) and 150mA output current. The SCT71401 series products is stable with 3.3uF~220uF output capacitors, and 10uF ceramic capacitor is recommended.

Only 2.5-µA typical quiescent current at light load makes the SCT71401 series products ideal choices for portable devices with battery power supply and an optional solution for powering microcontrollers (MCUs) and CAN/LIN transceivers in always-on systems.

The SCT71401 series products integrated short-circuit and overcurrent protection with OCFB (Over Current Fold-back) feature, which makes the device more reliable during transient high-load current faults or shorting events.

The SCT71401 series products provide fixed 3.3V and 5V output voltage versions, and also could provide 1.2V, 1.8V, 2.5V, 3V, 4.2V and 4.5V fixed output voltage versions, please contact SCT sales if needed.

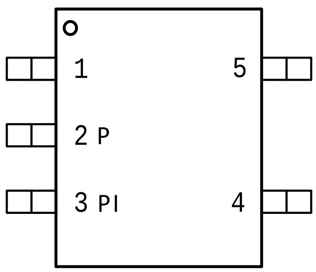
The SCT71401 series products is available in SOT23-5L and SOT23-3L packages, for other package options, please contact SCT sales.



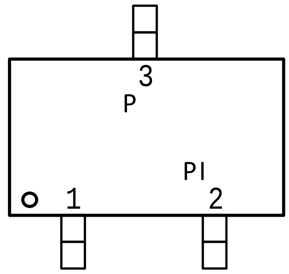
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to production.
Revision 1.1: Update the thermal information and the thermal characteristic.
Revision 1.2: Update the thermal information and the thermal characteristic.
Revision 1.3: Update the TAPE AND REEL INFORMATION.
Revision 1.4: Update DEVICE ORDER INFORMATION and TAPE AND REEL INFORMATION.
Revision 1.5: Remove one package type.

SCT71401F50TWDR	Fixed 5.0V	SOT23-5L	1F50	5	3	Tape & Reel, 3000
SCT71401F33TWDR	Fixed 3.3V	SOT23-5L	1F33	5	3	Tape & Reel, 3000
SCT71401F50TYDR	Fixed 5.0V	SOT23-3L	1F50	3	3	Tape & Reel, 3000
SCT71401F33TYDR	Fixed 3.3V	SOT23-3L	1F33	3	3	Tape & Reel, 3000



SOT23-5L Package



SOT23-3L Package

Over operating free-air temperature range unless otherwise noted

V_{IN}	Input voltage range	3	40	V
V_{OUT}	Output voltage range	1.2	5	V
C_{IN}	Input capacitor	2.2	--	uF
C_{OUT}				

V_{IN}=V_{OUT}+1V, C_{OUT}=10uF, T_J= -40°C~125°C, typical value is tested under 25°C.

V_{IN}	Operating input voltage		3 40	V
V_{UVLO}	V_{IN} UVLO Threshold	V_{IN} rising	2.3	

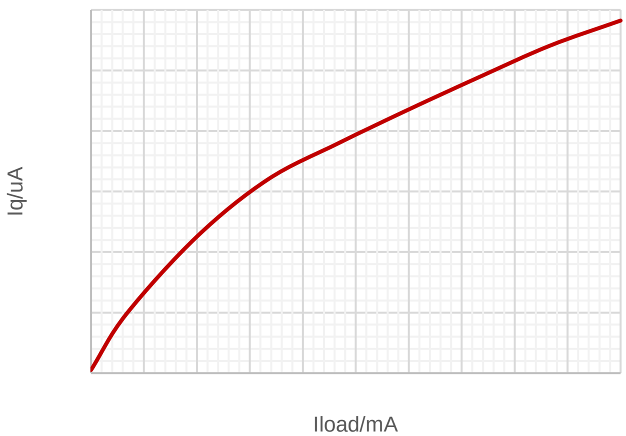


Figure 1. Quiescent Current vs Output Current

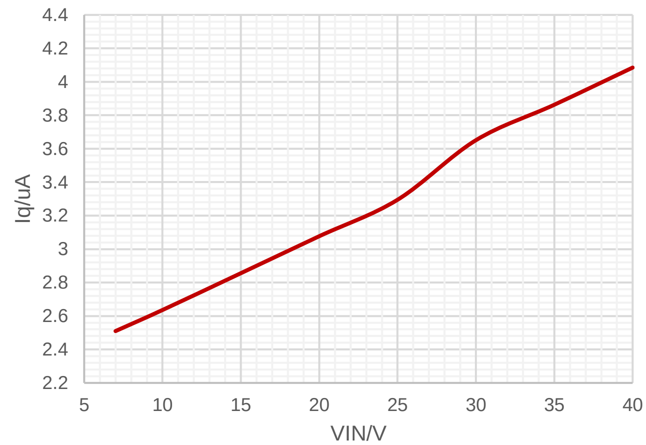


Figure 2. Quiescent Current vs Input Voltage, No load

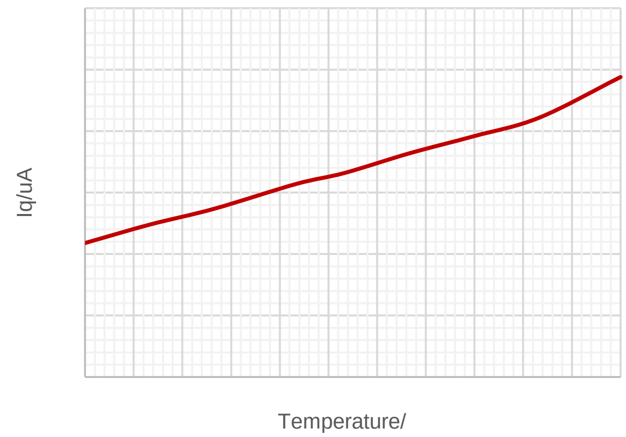


Figure 3. Quiescent Current vs Ambient Temperature

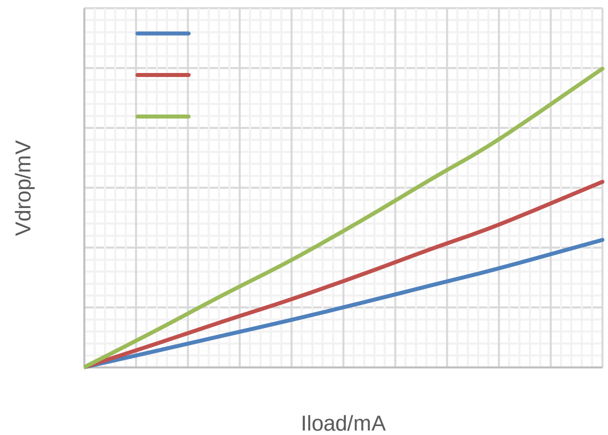


Figure 4. Dropout Voltage vs Output Current

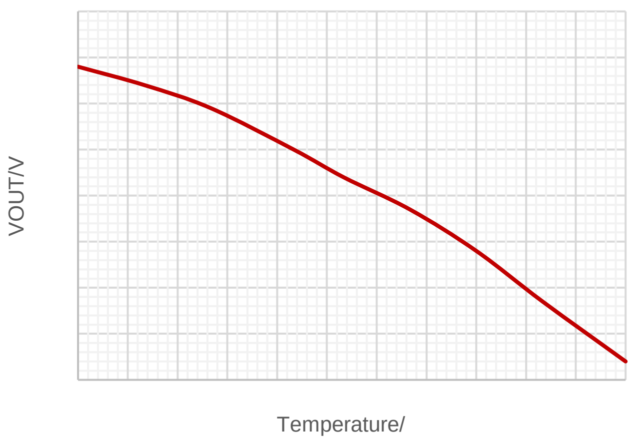


Figure 5. Output Voltage vs Ambient Temperature at VOUT=5V

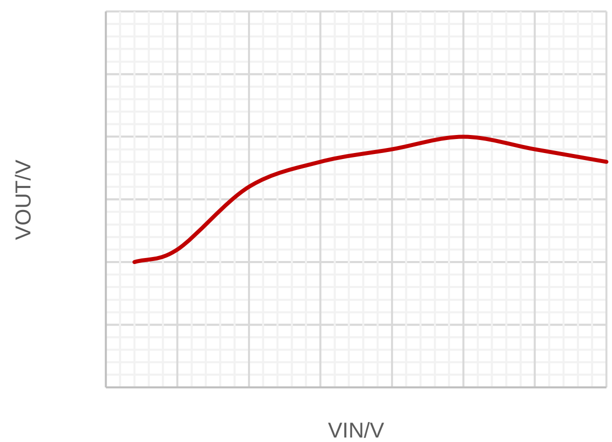


Figure 6. Output Voltage vs Input Voltage

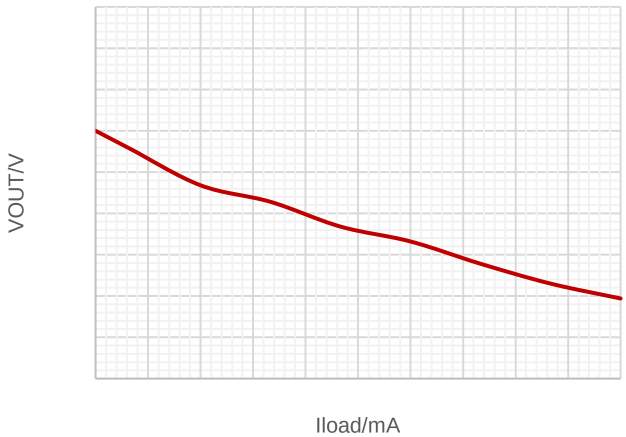


Figure 7. Output Voltage vs Output Current at VOUT=5V

Figure 8. Output Voltage vs Output Current at VOUT=3.3V

Figure 9. Output Current Limit vs Ambient Temperature at VIN<30V

Figure 10. Output Current Limit vs Ambient Temperature at VIN 30V

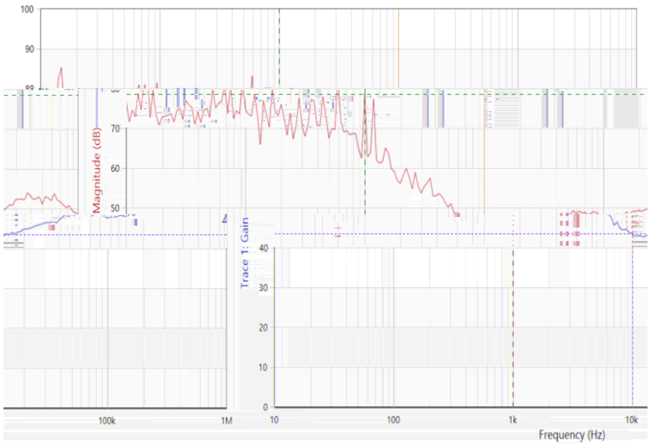


Figure 11. PSRR vs Frequency at Iout=10mA, C_{OUT}=4.7uF

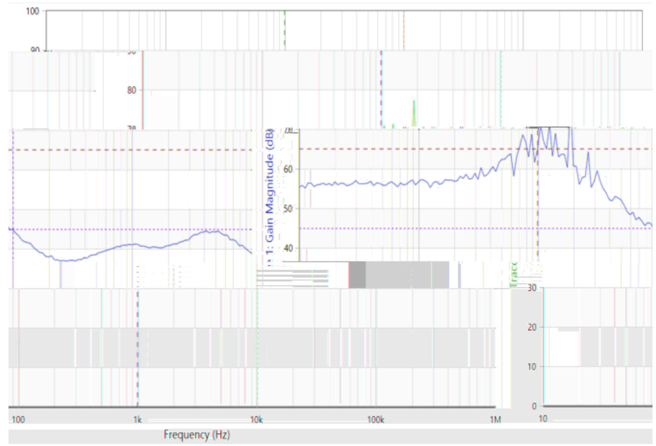


Figure 12. PSRR vs Frequency at Iout=100mA, C_{OUT}=4.7uF

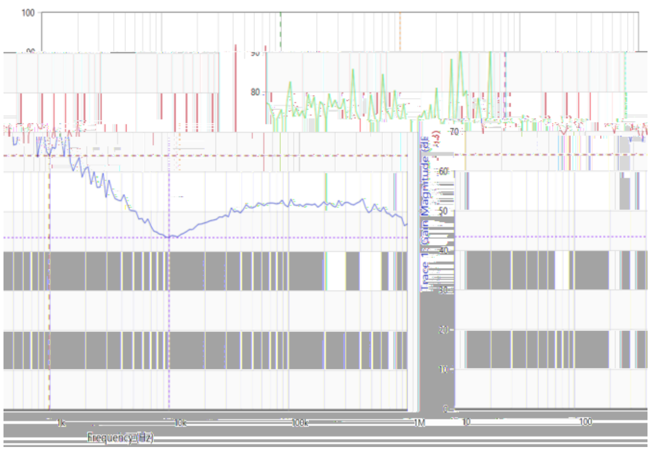


Figure 13. PSRR vs Frequency at Iout=10mA, C_{OUT}=10uF

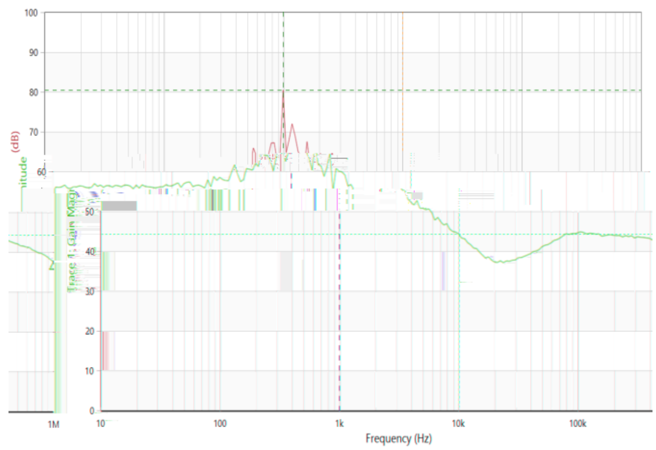


Figure 14. PSRR vs Frequency at Iout=100mA, C_{OUT}=10uF

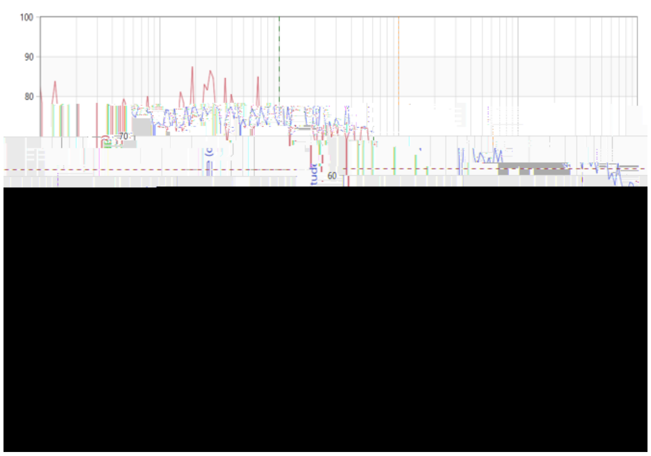


Figure 15. PSRR vs Frequency at Iout=10mA, C_{OUT}=22uF

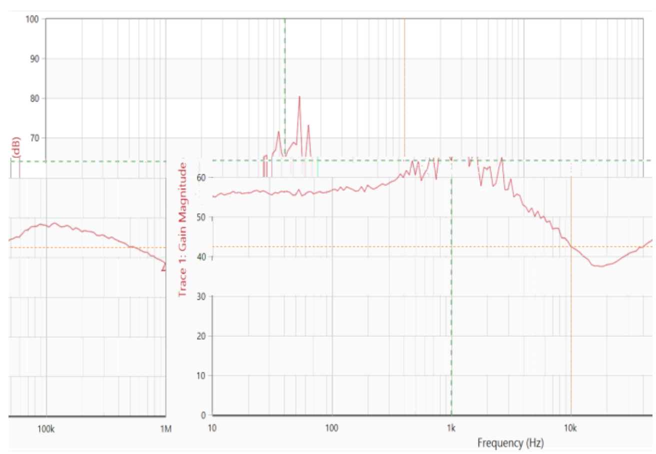


Figure 16. PSRR vs Frequency at Iout=100mA, C_{OUT}=22uF

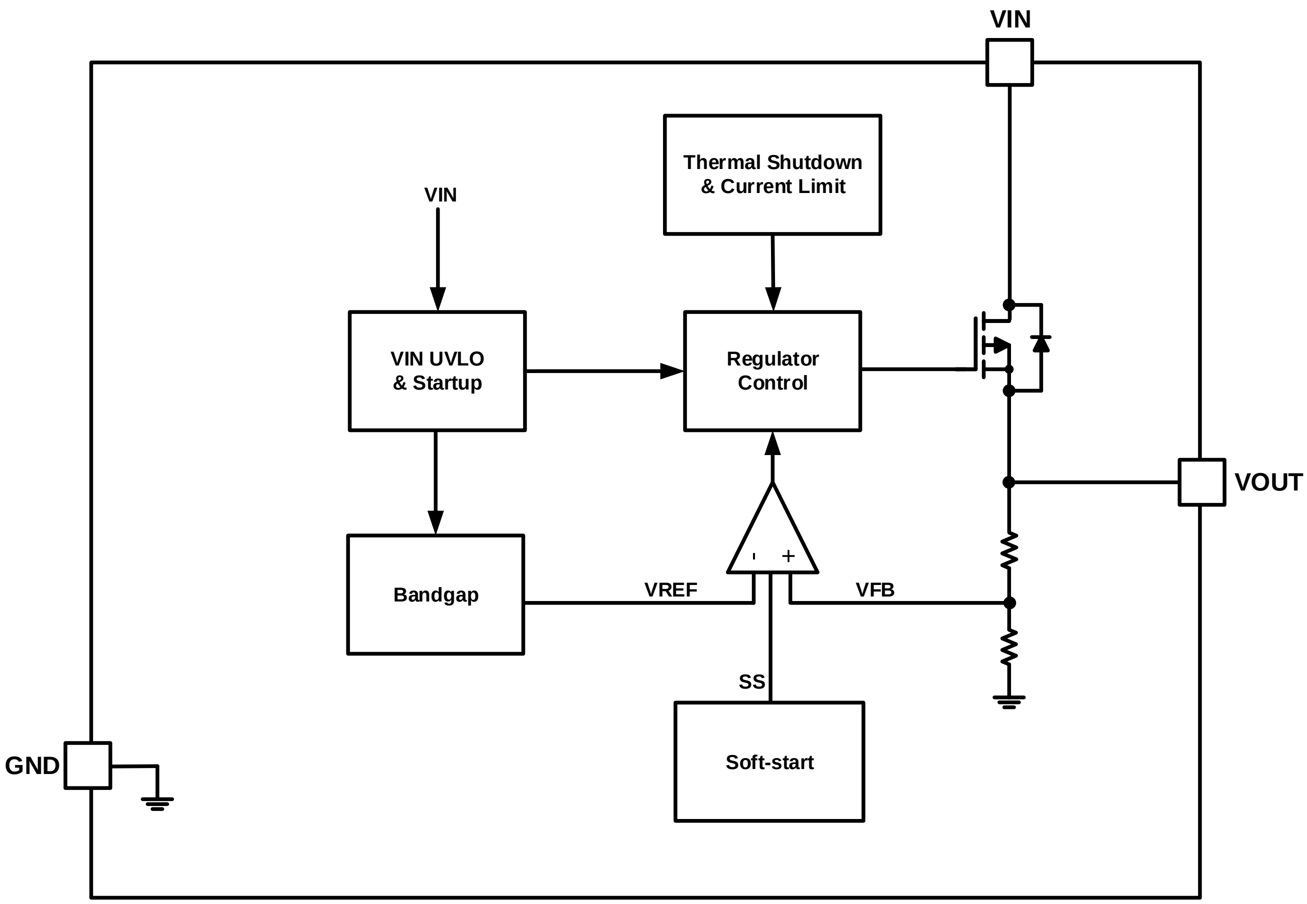


Figure 17. Functional Block Diagram

The SCT71401 series products are 150mA wide input voltage range linear regulators with very low quiescent current. These voltage regulators operate from 3V to 40V DC input voltage with supporting 45V transient input voltage and consume 2.5μA quiescent current at no load.

The SCT71401 series products is stable with 3.3uF~220uF output capacitors, and 10uF ceramic capacitor is recommended. An internal 660us soft-start time avoids large inrush current and output voltage overshoot during startup.

The SCT71401 series products also provide the VIN input under-voltage lockout, over current protection, output hard short protection and thermal shutdown protection.

The SCT71401 series products are available in fixed voltage versions of 3.3V and 5V with 1% output voltage accuracy at room temp and 2% output voltage accuracy over operating conditions. The series products are available in SOT23-5L and SOT23-3L packages.

The SCT71401 series are available in fixed voltage versions of 3.3V and 5V. When the input voltage is higher than $V_{OUT(NOM)}+V_{DROP}$, output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT(NOM)}+V_{DROP}$, output pin tracks the input voltage minus the dropout voltage based on the load current. When the input voltage drops below UVLO threshold, the output keeps shut off.

The SCT71401 series products also could provide other fixed output voltage versions of 1.2V, 1.8V, 2.5V, 3V, 4.2V and 4.5V and other package options. Please feel free to contact SCT sales, if you need a new output voltage version or a new package option.

The SCT71401 series products has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is 300mA when VIN<30V, but SCT71401 supplies a fold-back current limit 100mA when VIN>30V.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the regulator begins to heat up because of the increase in power dissipation. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition persists, the device cycles between current limit and thermal shutdown.

With the over current foldback limit feature, the SCT71401 series products would be more robust and safer when over current faults and shorting events occur. But it also requires the maximum loading current should be smaller than Isc during startup. The characteristic is shown in the following figure.

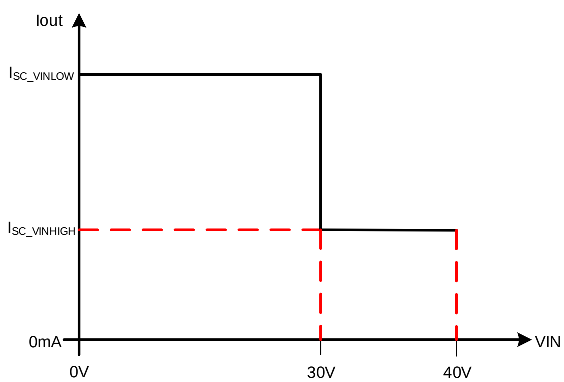


Figure 18. Current Limit with Foldback Feature

The SCT71401 series products integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.6V reference voltage in 660us. The soft-start will reset during shutdown due to thermal overloading.

Below figure shows the startup waveform at small output capacitor and large output capacitor. When output capacitor is small, for example 10uF, the slope of VOUT is limited by soft-start. When output capacitor is large, for example 100uF, the slope of VOUT is limited by current limit (I_{SC_VINLOW}) at VIN<30V, and the slope of VOUT is limited by current limit ($I_{SC\_VINHIGH}$), when VIN> 30V.

In SCT71401 series products, typical Tss is 660us, and typical I_{SC_VINLOW} is 300mA and typical $I_{SC\_VINHIGH}$ is 100mA, could use the following formula for initial startup time calculation.

$$\mathrm{d} \quad \mathrm{d} \qquad \overline{} \quad _{cc} \tag{1}$$

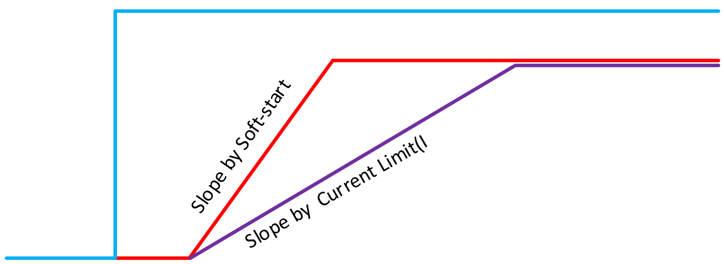


Figure 19. Soft-start Waveform vs Output Capacitor

This device incorporates a thermal shutdown (T_{SD}) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the T_{SD} trip point. The junction temperature exceeding the T_{SD} trip point causes the output to turn off. When the junction temperature falls below the T_{SD} trip point minus thermal shutdown hysteresis, the output turns on again.

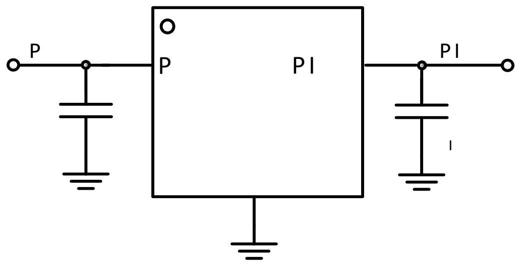


Figure 20. SCT71401 Typical Application Schematic

In some applications, the VIN and the VOUT potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, the accumulated charge in the output pin capacitor flowing backward from the VOUT to the VIN when the VIN shorts to the GND. In order to minimize the damage in such case, use a capacitor with a capacitance less than 220µF. Also by inserting a reverse polarity diode in series to the VIN, it can prevent reverse current from reverse battery connection or the case, when the point A is short-circuited GND. If there may be any possible case point B is short-circuited to GND, we also recommend using a bypass diode between the VIN and the VOUT.

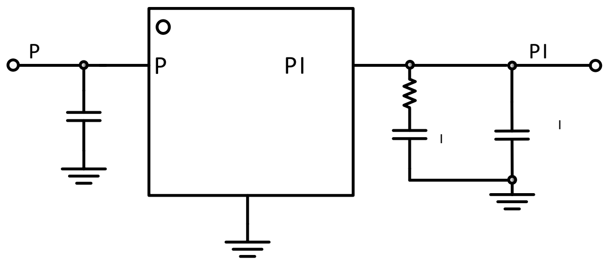


Figure 22. SCT71401 Typical Application Schematic with Large Output Capacitor

Input Voltage	12V Normal, 5.5V~40V
Output Voltage	5V or 3.3V
Maximum Output Current	150mA
Output Capacitor Range (C_{OUT1} and ESR)	3.3uF~220uF with ESR=0.5Ω~5Ω
Output Capacitor Range (C_{OUT2})	recommends 10uF with low ESR
Input Capacitor Range (C_{IN})	>2.2uF , recommends 10uF

SCT recommends adding a 2.2µF or greater capacitor with a 0.1µF bypass capacitor in parallel at VIN pin to keep the input voltage stable. Aluminum electrolytic capacitor or other capacitor with high capacitance is suggested for the system power with large voltage spike. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the SCT71401 series products requires an output capacitor with a minimum effective capacitance value of 3.3µF. And the series products could support output capacitor range from 3.3uF to 220uF and with an ESR range between 0.001Ω and 5Ω. SCT recommends selecting a X5R- or X7R-type 4.7uF~10uF ceramic capacitor with low ESR over temperature range to improve the load transient response.

When using large output capacitor with higher ESR resistor, for example 100uF output electrolytic capacitor with 1Ω ESR resistor in the application, SCT recommends adding extra 10uF low ESR output capacitor parallel connection with the large electrolytic capacitor, this will eliminate the undershoot/overshoot voltage caused by the large ESR resistor and get better load transient performance.

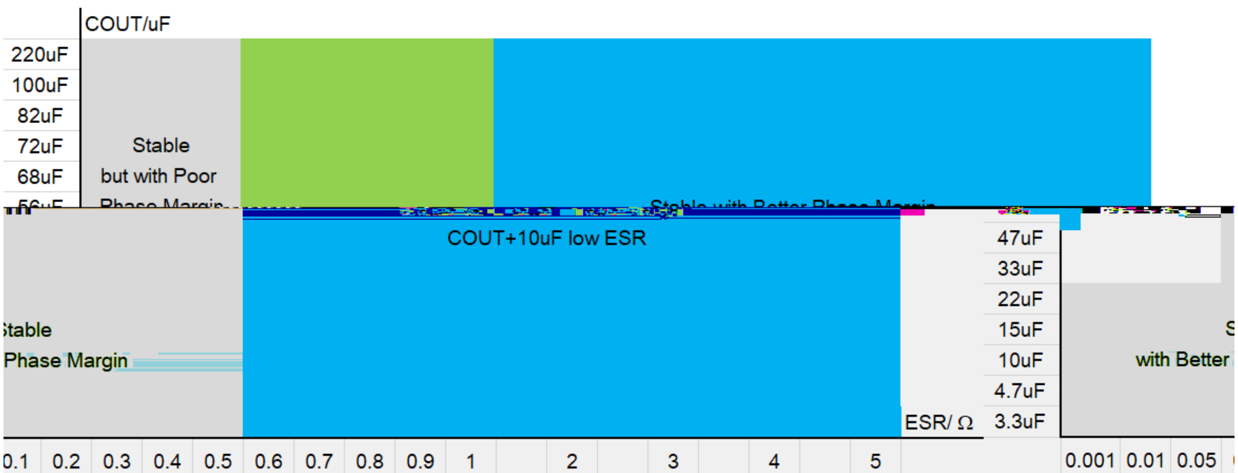


Figure 23. SCT71401 Stability vs Output Capacitor

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum junction temperature is dependent on power dissipation, package, the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature.

During normal operation, LDO junction temperature should not exceed 150°C, or else it may result in deterioration of the properties of the chip. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 2. Because $I_{GND} \ll I_{OUT}$, the term V_{IN} x I_{GND} in Equation 2 could be ignored.

$$ED \quad ED \tag{2}$$

The junction temperature can be estimated using Equation 3. $R_{\theta JA\_EVM}$ is the junction-to-ambient thermal resistance based on customer's PCB. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature T_J.

(3)

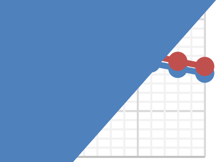
$R_{\theta JA\_EVM}$ is a critical parameter and depends on many factors such as the following:

• Power dissipation
• Air temperature/flow
• PCB area
• Copper heat-sink area
• Number of thermal vias under the package
• Adjacent component placement

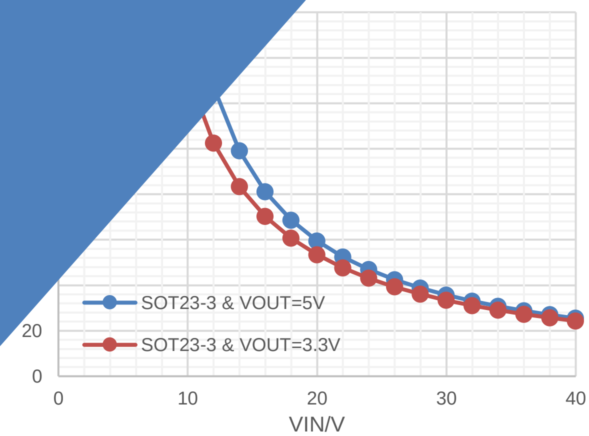
For the SCT71401 series products, the maximum allowable power dissipation of different packages was listed in the following table, and the test results are based on our EVM board, larger power dissipation will trigger thermal shutdown protection. As a result, we could calculate the R $_{JA\_EVM}$ of different packages. The following table is just for your reference based on our EVM test, please leave enough margin when you design thermal performance.

The PCB information of our EVM: 2-layer, 1oz Cu, 50mm x 30mm size.

			℃
SOT23-5L	1.397	0.963	103.81
SOT23-3L	1.293	0.891	112.18

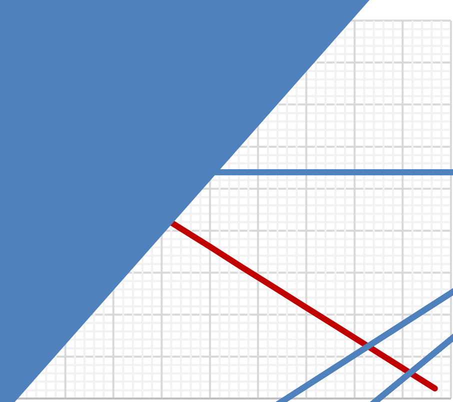


...nt vs Input Voltage,
...kages ,T_J ≤ TSD_R



...bient

Figure 27. Maximum Output Current vs Input Voltage, SOT23-3L,T_J 125



...8. Maximum Allowed Power Dissipation vs Ambient Temperature, SOT23-5L,T_J 125

Figure 29. Maximum Output Current vs Input Voltage, SOT23-5L,T_J 125

Vin=Vout +1V, unless otherwise noted

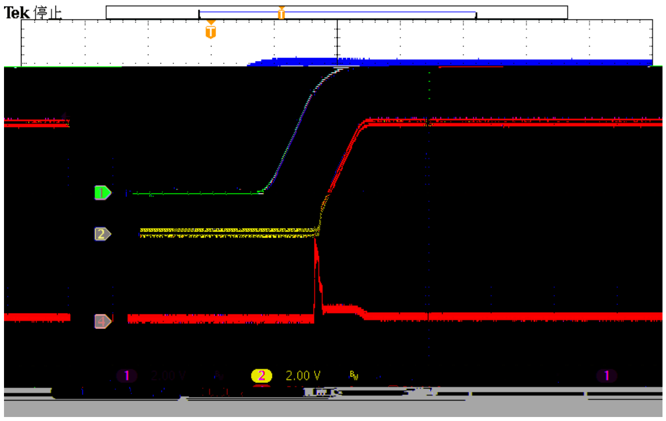


Figure 32. Power up (Iload=10mA)

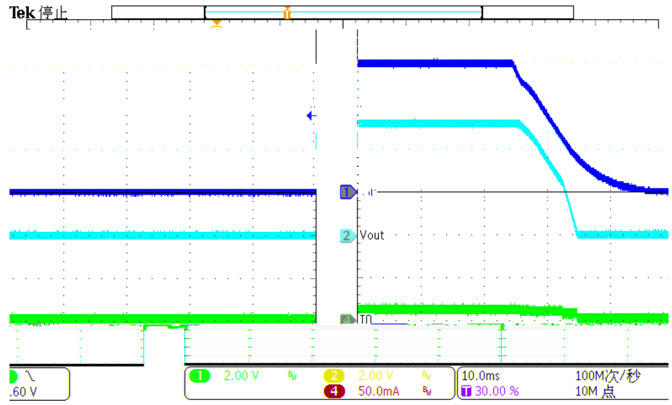


Figure 33. Power down (Iload=10mA)

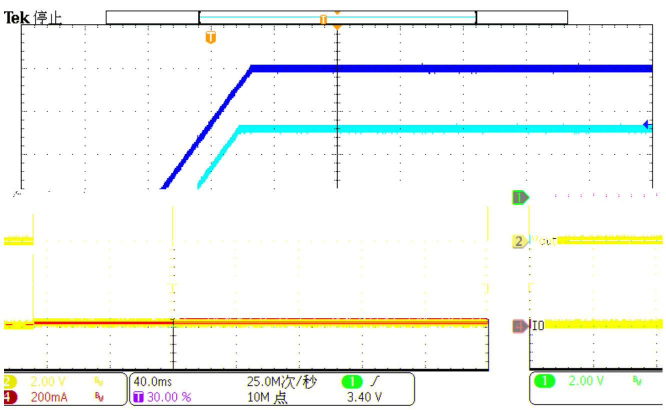


Figure 34. Slow Power up (Iload=10mA)

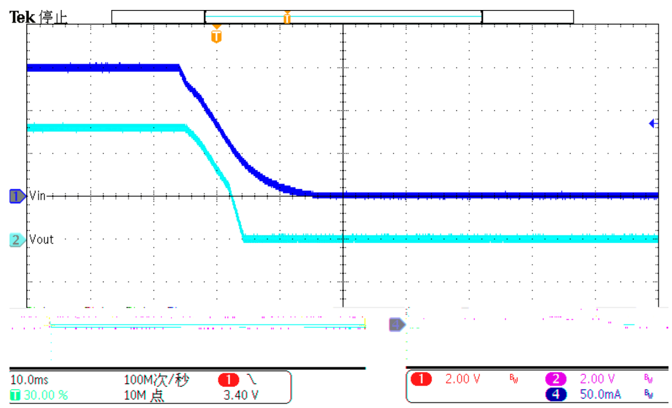


Figure 35 Slow Power down (Iload=10mA)

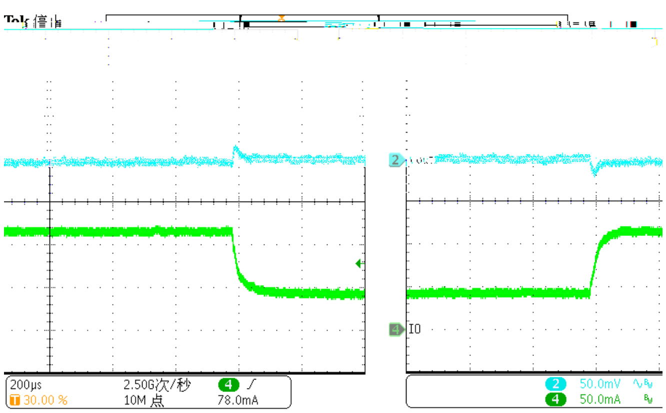


Figure 36. DC-DC Load Transient

(40mA-110mA),VOUT=5V

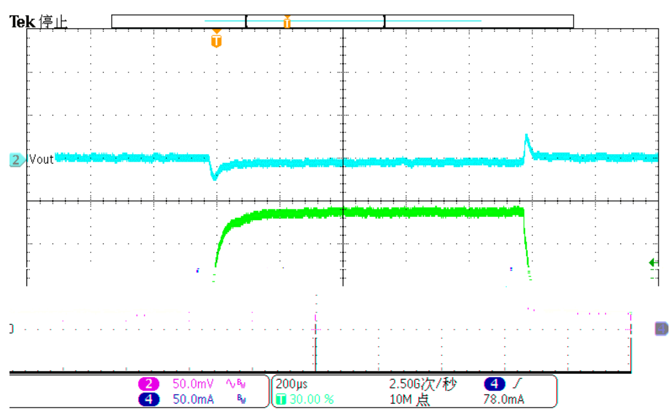


Figure 37. DC-DC Load Transient

(20mA-130mA),V_{OUT}=5V

Vin=Vout +1V, unless otherwise noted

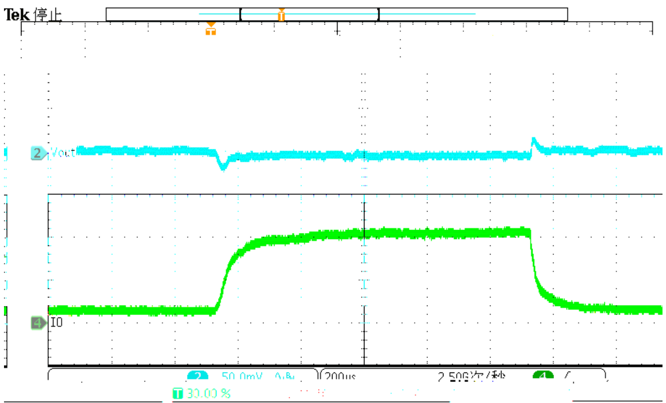


Figure 38. DC-DC Load Transient

(10mA-100mA),VOUT=5V

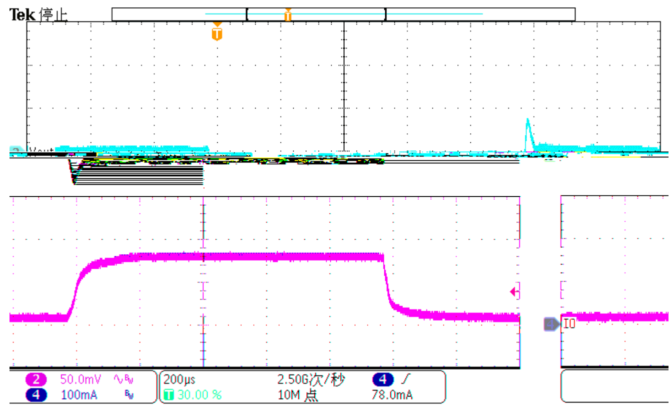


Figure 39. DC-DC Load Transient

(10mA-150mA),V_{OUT}=5V

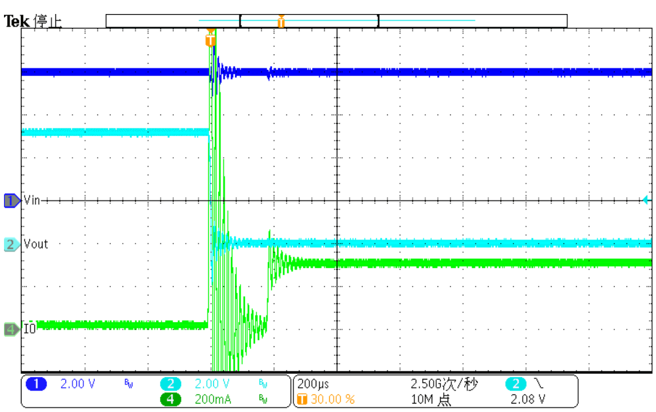


Figure 40. Enter Short Circuit Protection

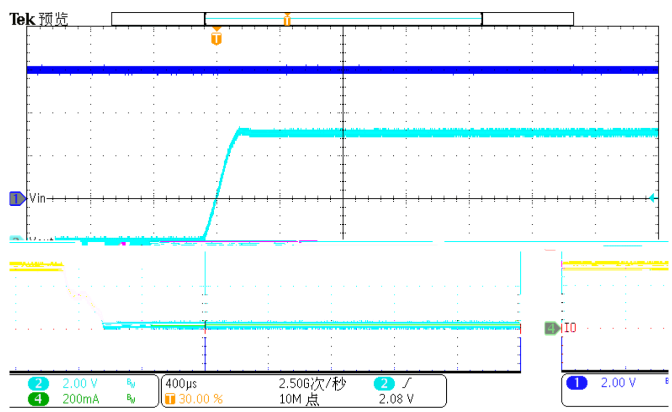


Figure 41 Exit Short Circuit Protection

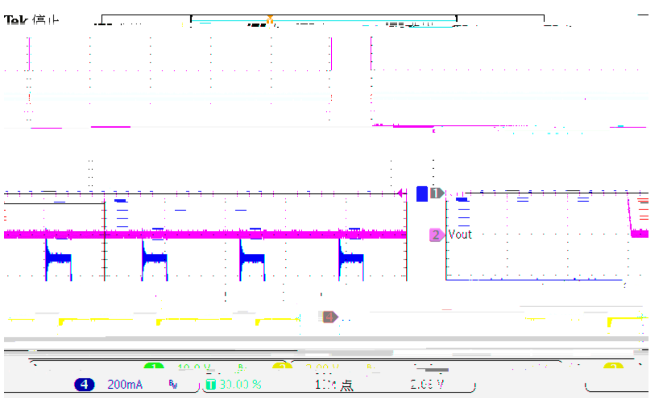


Figure 42. Enter Over Temperature Protection

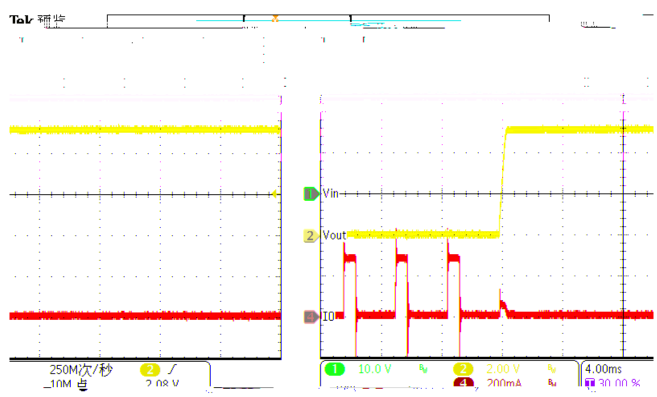
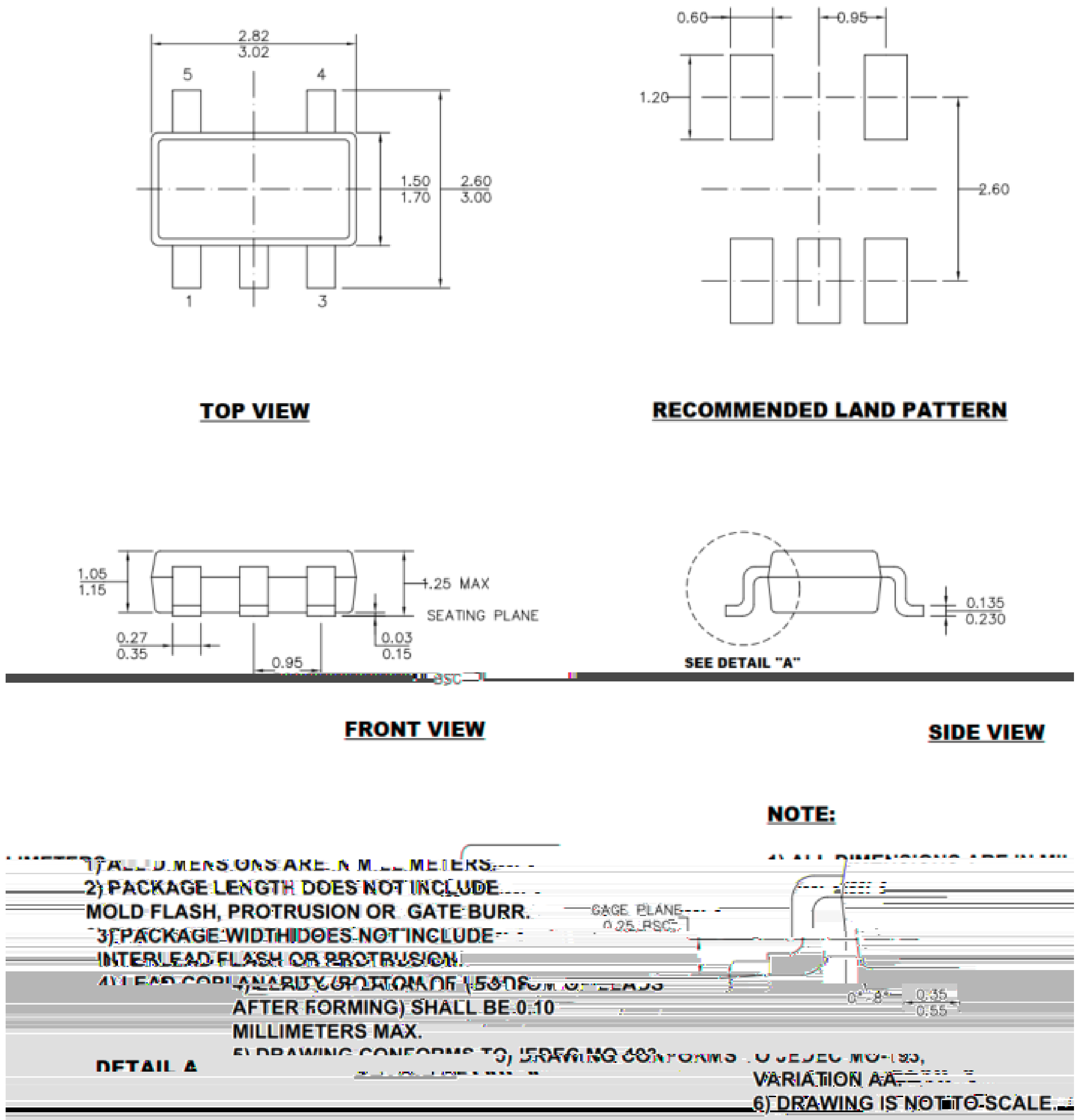


Figure 43. Exit Over Temperature Protection

Proper PCB layout is a critical for SCT71401's stability, transient performance and good regulation characteristics. For better results, follow these guidelines as below:

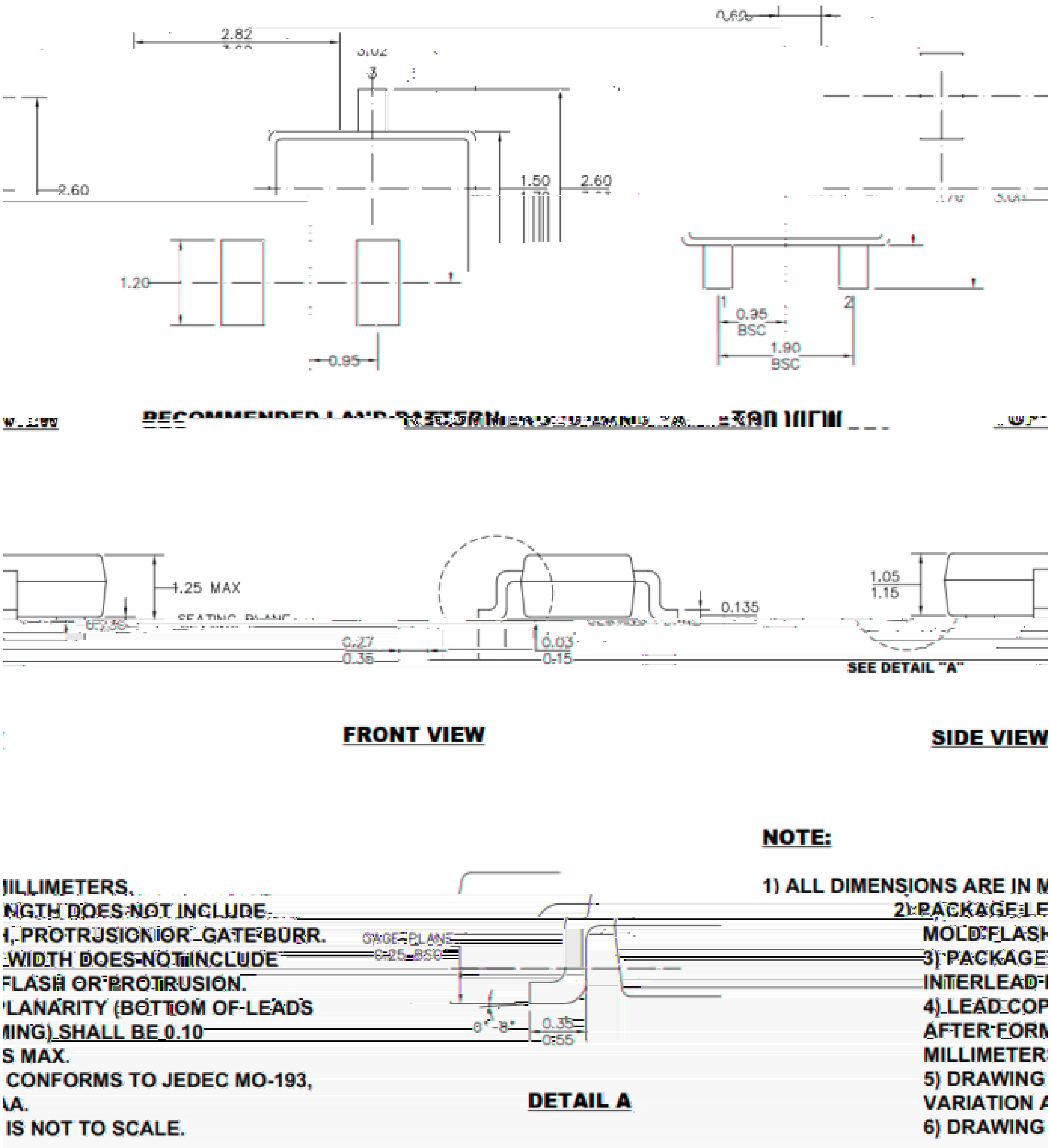
1. Both input capacitors and output capacitors must be placed as close to the device pins as possible.
2. It is recommended to bypass the input pin to ground with a 0.1µF bypass capacitor. The loop area formed by the bypass capacitor connection, V_{IN} pin and the GND pin of the system must be as small as possible.
3. It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.
4. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, SCT recommends spreading the copper under the thermal pad as far as possible and placing enough thermal vias on the copper under the thermal pad.
5. If using large electrolytic capacitor with high ESR resistor, SCT

Eh therma tibee l



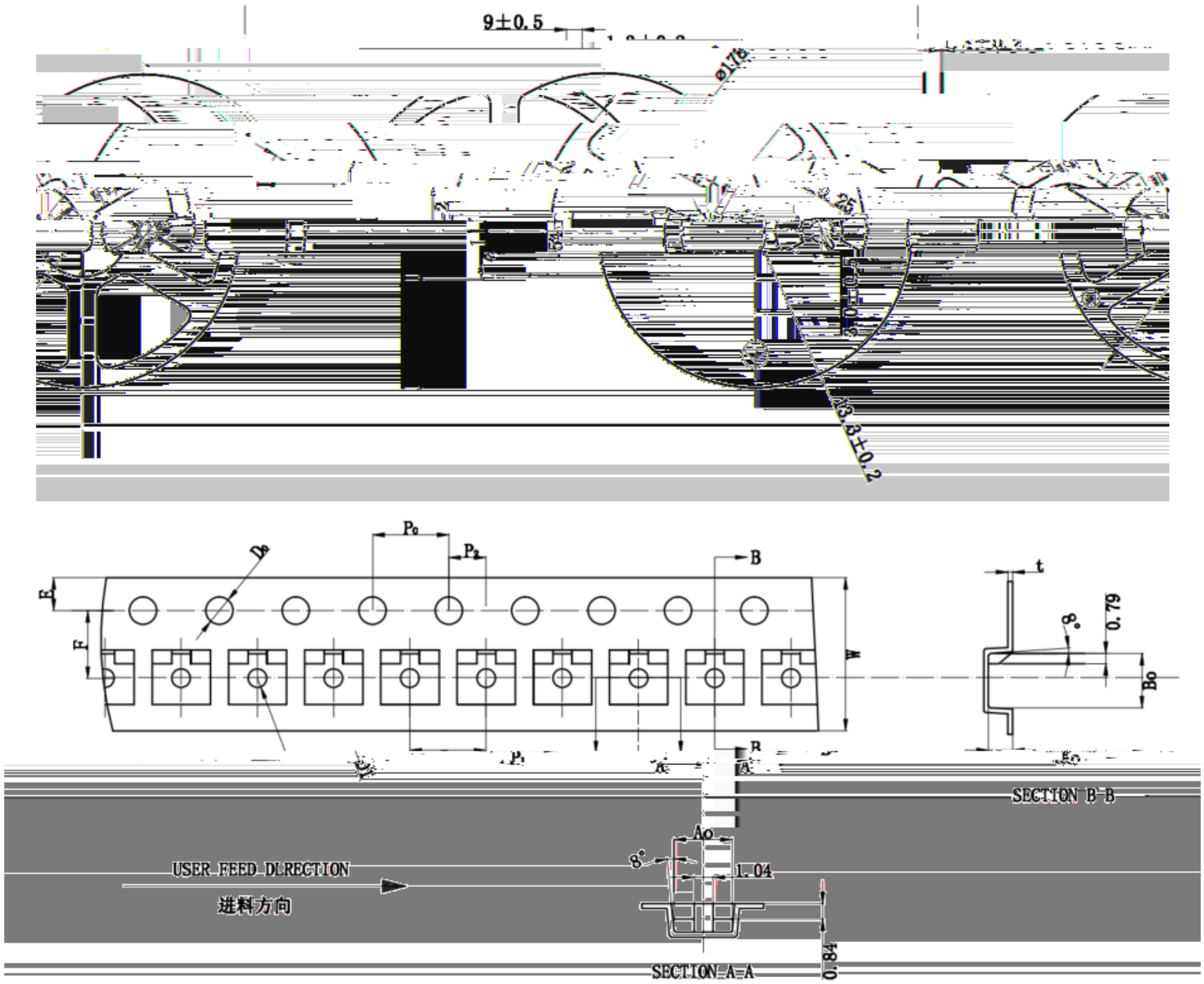
SOT23-5L Package Outline Dimensions

1. Drawing proposed to be made a JEDEC package outline MO-193 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.



SOT23-3L Package Outline Dimensions

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.



ITEM	W	Ao	Bo	Ko	E	F	D1	D₀	P₀	P₁	P₂	t
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

注：

1、任意10个齿轮的累计误差不超过±0.2m

2、材料厚度以载带边缘测量为准；

3、载带长度方向100mm距离的非平行度不可超过1mm；超过250mm不计算累计误差；

4、非指明，公差范围为：[illegible]

5、A₀、B₀为型腔内侧最底部向上0.3mm处测量为准；K₀为内部深度；

6、型腔外形凡未标明处倒角R为0.2~0.3

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