

**SCT2334U**

# SCT2334U

. / 4% 0 AGE NUMBERS FOR PREVIOUS REVISIONS MAY DIFFER FROM PAGE NUMBERS IN THE CURRENT VERSION  
2 EVISION      USTOMER3 AMPIES

| ORDERABLE<br>DEVICE | PACKAGING<br>TYPE | STANDARD<br>PACK QTY | PACKAGE<br>MARKING | PINS | PACKAGE<br>DESCRIPTION | MSL |
|---------------------|-------------------|----------------------|--------------------|------|------------------------|-----|
| 3 4      544 2      | 4APE 2EEL         |                      | 5                  |      | & 3/ 4                 | 4   |

/ VEROPERATINGFREE AIRTEMPERATURE UNLESS OTHERWISE NOTED

|   |  |                                                                                                                                                                                                                                    |
|---|--|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| & |  | INTERNAL INPUT OF THE TRANS CONDUCTANCE ERROR AMPLIFIER 4 THE TAP OF EXTERNAL FEEDBACK RESISTOR DIVIDER FROM THE OUTPUT TO . SETS THE OUTPUT VOLTAGE 4 THE DEVICE REGULATES & VOLTAGE TO THE INTERNAL REFERENCE VALUE OF 6 TYPICAL |
|---|--|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

/ VERO PERATING FREE AIR TEMPERATURE RANGE UNLESS OTHERWISE NOTED

| PARAMETER      | DEFINITION                      | MIN | MAX | UNIT |
|----------------|---------------------------------|-----|-----|------|
| 6 <sub>1</sub> | INPUT VOLTAGE RANGE             |     |     | 6    |
| 6 / 54         | / INPUT VOLTAGE RANGE           |     |     | 6    |
| 4*             | / PERATING JUNCTION TEMPERATURE |     |     |      |

| PARAMETER      | DEFINITION                                                            | MIN | MAX | UNIT |
|----------------|-----------------------------------------------------------------------|-----|-----|------|
| 6 <sub>3</sub> | ( UMAN BODY - CDEL ( - PER . 3 ) * % % * 3<br>SPECIFICATION ALLPINS   |     |     | K6   |
|                | HARDED DEVICE - CDEL ( - PER . 3 ) * % % * 3<br>SPECIFICATION ALLPINS |     |     | K6   |

- (1) \* % % DOCUMENT \* %0 STATES THAT 6 ( - ALLOWS SAFE MANUFACTURING WITH A STANDARD %3 CONTROL PROCESS  
 (2) \* % % DOCUMENT \* %0 STATES THAT 6 - ALLOWS SAFE MANUFACTURING WITH A STANDARD %3 CONTROL PROCESS

| PARAMETER         | THERMAL METRIC                                    | FCSOT583 | UNIT |
|-------------------|---------------------------------------------------|----------|------|
| 2 *               | * JUNCTION TO AMBIENT THERMAL RESISTANCE          |          | 7    |
| *4                | * JUNCTION TO TOP CHARACTERIZATION PARAMETER      |          |      |
| *                 | * JUNCTION TO BOARD CHARACTERIZATION PARAMETER    |          |      |
| 2 * <sub>TP</sub> | * JUNCTION TO CASE THERMAL RESISTANCE             |          |      |
| 2 *               | * JUNCTION TO BOARD THERMAL RESISTANCE            |          |      |
| 2 * %6 -          | * JUNCTION TO AMBIENT THERMAL RESISTANCE %6 -     |          |      |
| *4 %6 -           | * JUNCTION TO TOP CHARACTERIZATION PARAMETER %6 - |          |      |

3 4 PROVIDES 2 \* AND 2 \* NUMBERS ONLY AS REFERENCE TO ESTIMATE JUNCTION TEMPERATURES OF THE DEVICES 2 \* AND 2 \* ARE NOT A CHARACTERISTIC OF PACKAGE ITSELF BUT OF MANY OTHER SYSTEM LEVEL CHARACTERISTICS SUCH AS THE DESIGN AND LAYOUT OF THE PRINTED CIRCUIT BOARD 0 ON WHICH THE 3 4 5 IS MOUNTED AND EXTERNAL ENVIRONMENTAL FACTORS 4 THE 0 BOARD IS A HEAT SINK THAT IS SOLDERED TO THE LEADS OF THE 3 4 5 HAVING THE DESIGN OR CONFIGURATION OF THE 0 BOARD CHANGES THE EFFICIENCY OF THE HEAT SINK AND THEREFORE THE ACTUAL 2 \* AND 2 \*

- MEASURED ON \* %3 LAYER 0 4 THE VALUES GIVEN IN THIS TABLE ARE ONLY VALID FOR COMPARISON WITH OTHER PACKAGES AND CANNOT BE USED FOR DESIGN PURPOSES 4 THESE VALUES WERE CALCULATED IN ACCORDANCE WITH \* %3 AND SIMULATED ON A SPECIFIED \* % % BOARD 4 THEY DO NOT REPRESENT THE PERFORMANCE OBTAINED IN AN ACTUAL APPLICATION

- MEASURED ON 3 4 STANDARD %6 - 3 4 5 EMO CARD / OUTER LAYER 0Z AND INNER LAYER 0Z COPPER THICKNESS MM X MM LAYER 0

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6) 6 4\* TYPICAL VALUE IS TESTED UNDER

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--------|-----------|----------------|-----|-----|-----|------|
|--------|-----------|----------------|-----|-----|-----|------|

## Power Supply

6) / PERATING INPUT VOLTAGE

6

| SYMBOL            | PARAMETER                                       | TEST CONDITION               | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------------------------------|------------------------------|-----|-----|-----|------|
| $f_{SW}$ - )      | - INIMUM SWITCHING FREQUENCY IN 53 - MODE       |                              |     |     |     | K( Z |
| $T_{ON}$ - )      | - INIMUM ON TIME                                |                              |     |     |     | NS   |
| $T_{OFF}$ - )     | - INIMUM OFF TIME                               |                              |     |     |     | NS   |
| $T_{AX}$ - 8      | - AX ON TIME                                    |                              |     |     |     | US   |
| <b>Power Good</b> |                                                 |                              |     |     |     |      |
| 60 56             | 0 OVERGOOD FLAG UNDERVOLTAGE TRIPPING THRESHOLD | POWER GOOD (% of FB voltage) |     |     |     |      |
|                   |                                                 | POWER BAD (% of FB voltage)  |     |     |     |      |
| 60 / 6            | 0 OVERGOOD FLAG OVERVOLTAGE TRIPPING THRESHOLD  | POWER BAD (% of FB voltage)  |     |     |     |      |
|                   |                                                 | POWER GOOD (% of FB voltage) |     |     |     |      |



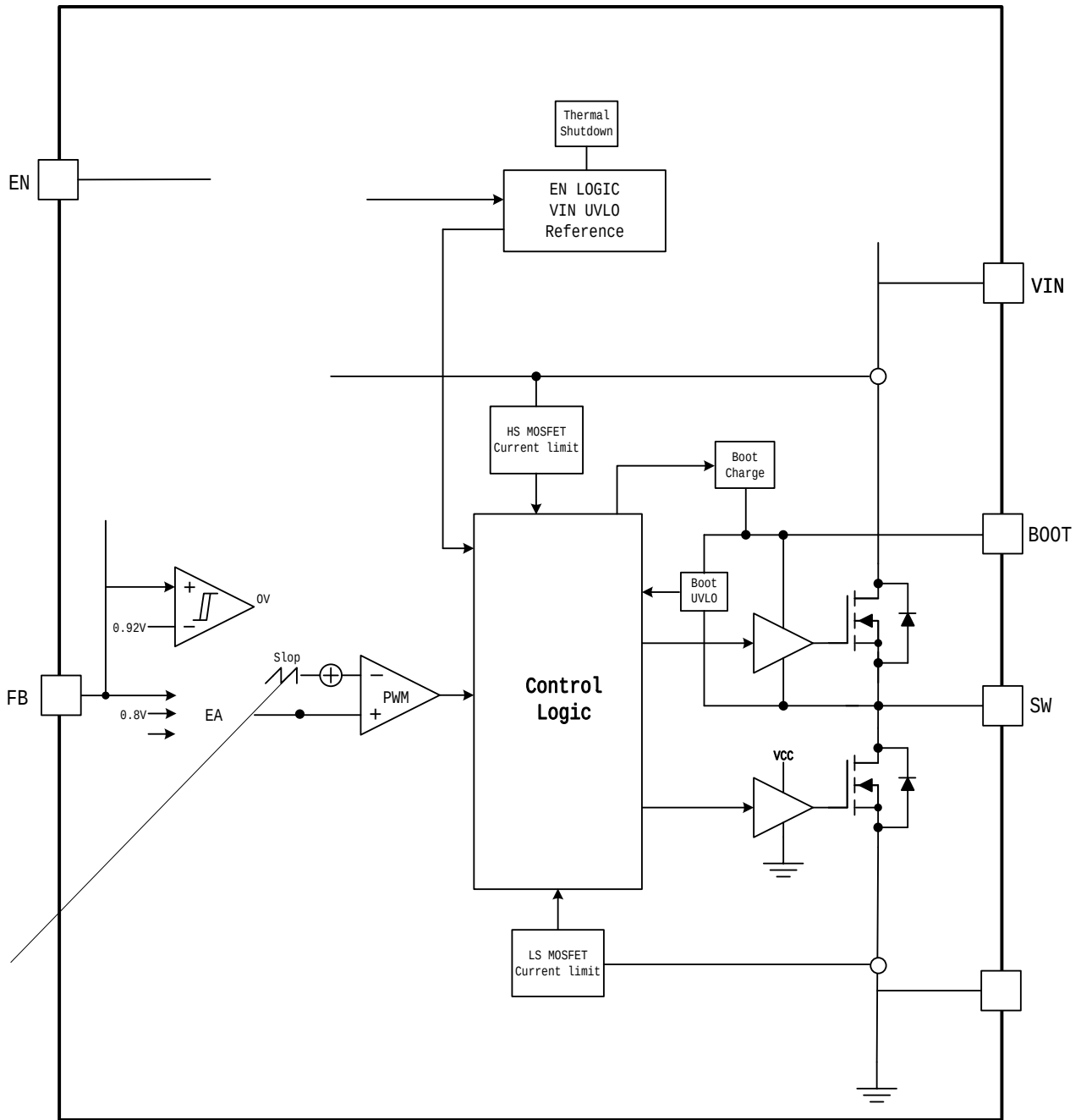


FIGURE 1 FUNCTIONAL BLOCK DIAGRAM

## Overview

The 345 is a 66 input/output friendly synchronous buck converter with built-in MOSFET high-side and MOSFET low-side power MOSFETs. It implements constant-frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is adjustable from kHz to MHz through resistor to optimize either the power efficiency or the external components sizes. The 345 features 1ms soft start time to avoid large inrush current. The device also supports monolithic startup with pre-biased output condition.

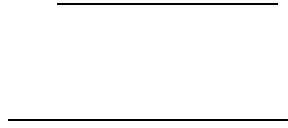
The % pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher 56V system requirements.

The 345 achieves random spread spectrum modulation expansion centered on the set switching frequency. The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading these emissions across a wide range of frequencies rather than apart with fixed frequency operation.

The 345 full protection features include the input undervoltage lockout, the output overvoltage protection, overcurrent protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

## Peak





7 HERE

6<sub>RSE</sub> IS RISING THRESHOLD OF 6 IN 56, /

6<sub>FAIL</sub> IS FALLING THRESHOLD OF 6 IN 56, /

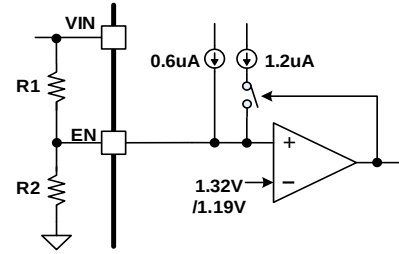
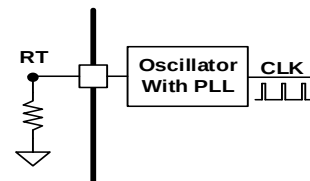


FIGURE 3 SYSTEM 56, / BY ENABLE DIMDE

### Output Voltage

4HE 3 4 5 REGULATES THE INTERNAL REFERENCE VOLTAGE AT 6 WITH TOLERANCE OVER THE OPERATING TEMPERATURE AND VOLTAGE RANGE 4HE OUTPUT VOLTAGE IS SET BY A RESISTOR DIVIDER FROM THE OUTPUT NODE TO THE & PIN ) IT IS RECOMMENDED TO USE TOLERANCE OR BETTER RESISTORS 5 SEE EQUATION TO CALCULATE RESISTANCE OF RESISTOR DIVIDERS 40

IN RESISTOR SETTING FREQUENCY MODE A RESISTOR PLACED BETWEEN 24 PIN TO THE GROUND SETS THE SWITCHING FREQUENCY OVER A WIDE RANGE FROM  $\frac{K}{Z}$  TO  $\frac{K}{Z} \times 7$  WHEN 24 IS FLOATING THE FREQUENCY IS  $\frac{K}{Z}$  AND WHEN 24 IS CONNECTED TO THE GROUND THE FREQUENCY IS  $\frac{K}{Z} \times 5$  SEE EQUATION OR THE PLOT IN FIGURE 3 TO DETERMINE THE RESISTANCE FOR A SWITCHING FREQUENCY NEEDED



WHERE  $f_{SW}$  IS SWITCHING CLOCK FREQUENCY

FIGURE 3 SETTING FREQUENCY AND LOCK SYNCHRONIZATION

## Frequency Spread Spectrum

TO REDUCE EMI THE SCT2334U IMPLEMENTS FREQUENCY SPREAD SPECTRUM. THE PURPOSE OF SPREAD SPECTRUM IS TO ELIMINATE PEAK EMISSIONS AT SPECIFIC FREQUENCIES BY SPREADING THESE EMISSIONS ACROSS A WIDER RANGE OF FREQUENCIES RATHER THAN A PART WITH FIXED FREQUENCY FUNCTION. IN MOST SYSTEMS CONTAINING THE SCT2334U LOW FREQUENCY CONDUCTED EMISSIONS FROM THE FIRST FEW HARMONICS OF THE SWITCHING FREQUENCY CAN BE EASILY FILTERED.

THE SCT2334U CIRCUIT USES PSEUDO RANDOM FREQUENCY HOPPING TO VARY THE SWITCHING FREQUENCY WITHIN A SPECIFIC RANGE. THE JITTERING SPAN IS 5% OF THE SWITCHING FREQUENCY. THE SPREAD SPECTRUM IS ONLY AVAILABLE WHILE THE CLOCK OF THE SCT2334U DEVICES IS FREE RUNNING AT THEIR NATURAL FREQUENCY. ANY OF THE FOLLOWING CONDITIONS OVERRIDES SPREAD SPECTRUM TURNING IT OFF.

- THE CLOCK IS REDUCED DURING, / FUNCTION
- THE CLOCK IS REDUCED AT LIGHT LOAD IN 53 -
- THE CLOCK IS REDUCED DURING MINIMUM ON TIME FUNCTION

## Bootstrap Voltage Regulator and BOOT UVLO

AN EXTERNAL BOOTSTRAP CAPACITOR BETWEEN / / 4 PIN AND 37 PIN POWERS THE FLOATING GATE DRIVER TO HIGH SIDE POWER. / 3 & %4 THE BOOTSTRAP CAPACITOR VOLTAGE IS CHARGED FROM AN INTEGRATED VOLTAGE REGULATOR WHEN HIGH SIDE POWER / 3 & %4 IS OFF AND LOW SIDE POWER / 3 & %4 IS ON. BOOT DIODE IS INTEGRATED ON THE 3 4 5 DIE.

### Minimum On Time Function

When the duty cycle at the set frequency is limited by the minimum on time, the device can still maintain stable adjustment of the output voltage during the transition from high input voltage to low output voltage.

If the input/output voltage ratio is too high, even if the current exceeds the compensation specified peak, the high side MOSFET cannot shutdown quickly enough to adjust the output voltage. This will cause the output voltage to continuously increase until overvoltage protection is triggered. To avoid this situation, when the conduction time of the high side MOSFET touches the minimum on time due to the increase in input and output voltage difference, the device will switch to valley current control mode. For the high side MOSFET, the low side MOSFET will remain open until the inductor current drops below the required valley current. During this period, the next clock cycle will be blocked from starting, so the switching frequency will decrease. Since the on time of high side MOSFET is fixed at its minimum value, this type of function resembles that of a device using a constant/variable control scheme.

### Over Current Limit and Hiccup Mode

The inductor current is monitored during high side MOSFET conduction and low side MOSFET conduction. The device implements over current protection with cycle by cycle limiting high side MOSFET peak current and low side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the inductor current is clamped at over current limitation. The converter cannot provide output current to satisfy loading requirement. Thus, the output capacitor is discharged and the output voltage drops below regulated voltage with a voltage less than internal reference voltage. Continuously, the output voltage ramps up to high clamp voltage when the voltage is below a certain percentage of the reference voltage and after a certain number of cycles of low side current limit, the converter stops switching. For remaining time, the device restarts from soft start phase. If overload or hard short condition still exists during this time, the output voltage is clamped at high after a certain time and the voltage keeps below a certain percentage of the reference voltage for a certain number of cycles. The device enters turning off mode again. When overload or hard short condition is removed, the device automatically recovers to enter normal regulating function.

If the output voltage drops below a certain percentage of the reference voltage due to, for example, function hiccup mode will be disabled.

The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

### Over voltage Protection

The device implements the overvoltage protection circuitry to minimize output voltage overshoot during load transient recovering from output fault condition or light load transient. The overvoltage comparator in the circuit compares the output pin voltage to the internal reference voltage. When the output voltage exceeds a certain percentage of internal reference voltage, the high side MOSFET turns off to avoid output voltage continue to increase. When the output pin voltage falls below a certain percentage of the internal reference voltage, the high side MOSFET can turn on again.

### Power Good

The PG pin is an open drain output. Connect the pin to a 5V or other voltage source through a pull up resistor between 10K and 100K. Please ensure that the voltage connected to the PG pin does not exceed 6V. Note the PG pin is between a certain percentage and a certain percentage of the internal voltage reference. The PG pin is deasserted and the pin floats with a 100ns delay. The PG pin is pulled low when the output voltage is lower than a certain percentage or greater than a certain percentage of the nominal internal reference voltage with a 100ns de-glitching time. Also, the PG pin is pulled low if a thermal shutdown is asserted or the PG pin is pulled low. Output voltage excursions that are shorter than 100ns de-glitching time do not trip the PG flag.

### Thermal Shutdown

The device protects the device from the damage during excessive heat and power dissipation conditions. Note the junction temperature exceeds a certain value, the internal thermal sensor stops power MOSFET switching. When the

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JUNCTION TEMPERATURE FALLS BELOW

THE DEVICE RESTARTS WITH INTERNAL SOFT START PHASE

## Typical Application

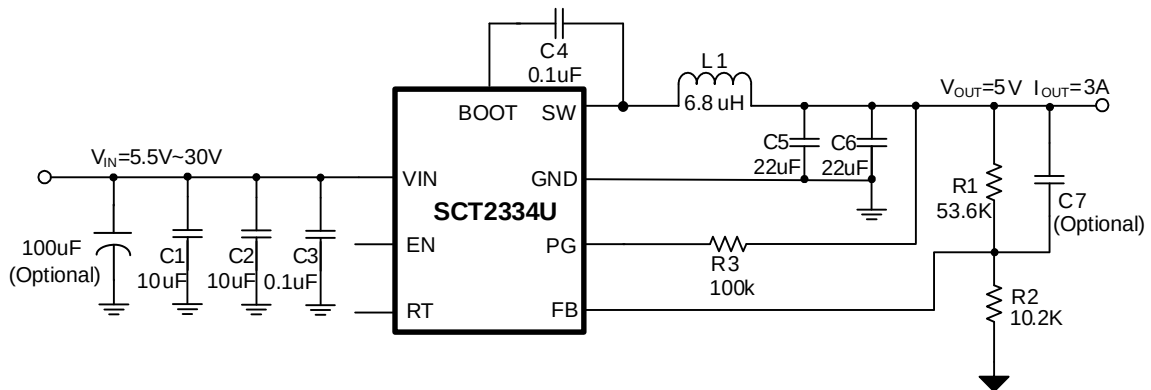


Figure 11. SCT2334U Design Example, 5V Output

## Design Parameters

| Design Parameters                  | Example Value |
|------------------------------------|---------------|
| INPUT VOLTAGE                      | 6.0V          |
| OUTPUT VOLTAGE                     | 6             |
| MAXIMUM OUTPUT CURRENT             |               |
| SWITCHING FREQUENCY                | KHz           |
| OUTPUT VOLTAGE RIPPLE PEAK TO PEAK | mV            |
| TRANSIENT RESPONSE TO LOAD STEP    | mV            |

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## Output Voltage

THE OUTPUT VOLTAGE IS SET BY AN EXTERNAL RESISTOR DIVIDER  $R_1$  AND  $R_2$  IN TYPICAL APPLICATION SCHEMATIC. RECOMMENDED RESISTANCE IS 5K. SEE EQUATION TO CALCULATE  $V_{OUT}$ .

| $V_{OUT}$ | $R_1$ | $R_2$ |
|-----------|-------|-------|
| 6         | +     | 5K    |
| 6         | +     | 5K    |
| 6         | +     | 5K    |

WHERE

$V_{FB}$  IS THE FEEDBACK REFERENCE VOLTAGE. TYPICAL 600mV.

## Switching Frequency

HIGHER SWITCHING FREQUENCIES SUPPORT SMALLER VALUES OF OUTPUT INDUCTORS AND OUTPUT CAPACITORS, RESULTING IN LOWER VOLTAGE AND CURRENT RIPPLES. HOWEVER, THE HIGHER SWITCHING FREQUENCY CAUSES EXTRA SWITCHING LOSS, WHICH DOWNGRADES CONVERTER OVERALL POWER EFFICIENCY AND THERMAL PERFORMANCE. IN THIS DESIGN, A MODERATE SWITCHING FREQUENCY OF 500KHz IS SELECTED TO ACHIEVE BOTH SMALL SOLUTION SIZE AND HIGH EFFICIENCY OPERATION.

Inductor value can be made smaller to reduce output ripple. In this example, 500KHz is selected.

4 THE TOTAL CURRENT FLOWING THROUGH THE INDUCTOR IS THE INDUCTOR RIPPLE CURRENT PLUS THE OUTPUT CURRENT 7 WHEN SELECTING AN INDUCTOR CHOOSE ITS RATED CURRENT ESPECIALLY THE SATURATION CURRENT LARGER THAN ITS PEAK OPERATION CURRENT AND 2-3 CURRENT ALSO NOT BE EXCEEDED 4 THEREFORE THE PEAK SWITCHING CURRENT OF INDUCTOR  $I_{L,0\%} +$  AND  $I_{L,2-3}$  CAN BE CALCULATED AS IN EQUATION AND EQUATION

$$I_{L,0\%} = \frac{V_{IN} - V_{OUT}}{L \cdot f_{SW}} \cdot D$$

$$I_{L,2-3} = \frac{V_{IN} - V_{OUT}}{L \cdot f_{SW}} \cdot (1 - D)$$

7 HERE

- $I_{L,0\%} +$  IS THE INDUCTOR PEAK CURRENT
- $I_{L,54}$  IS THE LOAD CURRENT
- $I_{L,00}$  IS THE INDUCTOR PEAK TO PEAK CURRENT
- $I_{L,2-3}$  IS THE INDUCTOR 2-3 CURRENT

IN OVERLOADING OR LOAD TRANSIENT CONDITIONS THE INDUCTOR PEAK CURRENT CAN INCREASE UP TO THE SWITCH CURRENT LIMIT OF THE DEVICE WHICH IS TYPICALLY 4 THE MOST CONSERVATIVE APPROACH IS TO CHOOSE AN INDUCTOR WITH A SATURATION CURRENT RATING GREATER THAN BECAUSE OF THE MAXIMUM  $I_{L,0\%} +$  LIMITED BY DEVICE THE MAXIMUM OUTPUT CURRENT THAT THE 3 4 5 CAN DELIVER ALSO DEPENDS ON THE INDUCTOR CURRENT RIPPLE 4 HUS THE MAXIMUM DESIRED OUTPUT CURRENT ALSO AFFECTS THE SELECTION OF INDUCTANCE 4 THE SMALLER INDUCTOR RESULTS IN LARGER INDUCTOR CURRENT RIPPLE LEADING TO A LOWER MAXIMUM OUTPUT CURRENT

### Input Capacitor Selection

4 THE INPUT CURRENT TO THE STEP DOWN CONVERTER IS DISCONTINUOUS THEREFORE IT REQUIRES A CAPACITOR TO SUPPLY THE CURRENT TO THE STEP DOWN CONVERTER WHILE MAINTAINING THE INPUT VOLTAGE 5 SE CAPACITORS WITH LOW  $\% \Delta C$  2 FOR BETTER PERFORMANCE CERAMIC CAPACITORS WITH  $\pm 2\%$  OR  $\pm 5\%$  DIELECTRICS ARE USUALLY SUGGESTED BECAUSE OF THEIR LOW  $\% \Delta C$  2 AND SMALL TEMPERATURE COEFFICIENTS AND IT IS STRONGLY RECOMMENDED TO USE ANOTHER LOWER VALUE CAPACITOR E.G. U8 WITH SMALL PACKAGE SIZE TO FILTER HIGH FREQUENCY SWITCHING NOISE 0 PLACE THE SMALL SIZE CAPACITOR AS CLOSE TO 6) AND 7 PINS AS POSSIBLE

4 THE VOLTAGE RATING OF THE INPUT CAPACITOR MUST BE GREATER THAN THE MAXIMUM INPUT VOLTAGE AND THE CAPACITOR MUST ALSO HAVE A RIPPLE CURRENT RATING GREATER THAN THE MAXIMUM INPUT CURRENT RIPPLE 4 THE 2-3 CURRENT IN THE INPUT CAPACITOR CAN BE CALCULATED USING EQUATION

$$I_{C,2-3} = \frac{V_{IN} - V_{OUT}}{L \cdot f_{SW}} \cdot (1 - D)$$

4 THE WORST CASE CONDITION OCCURS AT 6)  $I_{C,6/54}$  WHERE

FOR SIMPLIFICATION CHOOSE AN INPUT CAPACITOR WITH AN 2-3 CURRENT RATING GREATER THAN HALF OF THE MAXIMUM LOAD CURRENT

7 WHEN SELECTING CERAMIC CAPACITORS IT NEEDS TO CONSIDER THE EFFECTIVE VALUE OF A CAPACITOR DECREASING AS THE BIAS VOLTAGE ACROSS A CAPACITOR INCREASING

4 THE INPUT CAPACITANCE VALUE DETERMINES THE INPUT RIPPLE VOLTAGE OF THE REGULATOR 4 THE INPUT VOLTAGE RIPPLE CAN BE CALCULATED USING EQUATION AND THE MAXIMUM INPUT VOLTAGE RIPPLE OCCURS AT DUTY CYCLE

$$\Delta V_{IN} = \frac{I_{C,2-3}}{C \cdot f_{SW}} \cdot (1 - D)$$

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FOR THIS EXAMPLE TWO 10  $\mu$ F 8 V CERAMIC CAPACITORS RATED FOR 6 V IN PARALLEL ARE USED AND A 10  $\mu$ F 16 V FOR HIGH FREQUENCY FILTERING CAPACITOR IS PLACED AS CLOSE AS POSSIBLE TO THE DEVICE PINS

IF YOU WANT TO MAKE THE 53- WORK MORE STABLE UNDER LOW DROPOUT HIGH DUTY CYCLE IT IS RECOMMENDED TO ADD A LARGE ELECTROLYTIC CAPACITOR TO THE INPUT TO STABILIZE THE INPUT VOLTAGE

## Bootstrap Capacitor Selection

10  $\mu$ F CERAMIC CAPACITOR MUST BE CONNECTED BETWEEN 1 / 4 PIN AND 37 PIN FOR PROPER OPERATION CERAMIC CAPACITOR WITH 8 V OR BETTER GRADE DIELECTRIC IS RECOMMENDED THE CAPACITOR SHOULD HAVE A 16 V OR HIGHER VOLTAGE RATING

## Output Capacitor Selection

THE SELECTION OF OUTPUT CAPACITOR WILL AFFECT OUTPUT VOLTAGE RIPPLE IN STEADY STATE AND LOAD TRANSIENT PERFORMANCE

THE OUTPUT RIPPLE IS ESSENTIALLY COMPOSED OF TWO PARTS / ONE IS CAUSED BY THE INDUCTOR CURRENT RIPPLE GOING THROUGH THE EQUIVALENT RESISTANCE OF THE OUTPUT CAPACITORS AND THE OTHER IS CAUSED BY THE INDUCTOR CURRENT RIPPLE CHARGING AND DISCHARGING THE OUTPUT CAPACITORS TO ACHIEVE SMALL OUTPUT VOLTAGE RIPPLE CHOOSE A LOW  $\text{ESR}$  OUTPUT CAPACITOR LIKE CERAMIC CAPACITOR OR CERAMIC CAPACITORS THE CAPACITANCE DOMINATES THE OUTPUT RIPPLE FOR SIMPLIFICATION THE OUTPUT VOLTAGE RIPPLE CAN BE ESTIMATED BY EQUATION DESIRED

7 HERE

IS THE OUTPUT VOLTAGE RIPPLE  
 $F_{37}$  IS THE SWITCHING FREQUENCY  
 $L$  IS THE INDUCTANCE OF INDUCTOR  
 $C_{54}$  IS THE OUTPUT CAPACITANCE  
 $V_{54}$  IS THE OUTPUT VOLTAGE  
 $V_{IN}$  IS THE INPUT VOLTAGE

UE TO CAPACITORS DEGRADING UNDER BIAS THE BIAS VOLTAGE CAN SIGNIFICANTLY REDUCE CAPACITANCE CERAMIC CAPACITORS CAN LOSE MOST OF THEIR CAPACITANCE AT RATED VOLTAGE THEREFORE LEAVE MARGIN ON THE VOLTAGE RATING TO ENSURE ADEQUATE EFFECTIVE CAPACITANCE TYPICALLY TWO 10  $\mu$ F CERAMIC OUTPUT CAPACITORS WORK FOR MOST APPLICATIONS

Table 3: Typical External Component Values

|  |  |  |  |  |  |  |  |
|--|--|--|--|--|--|--|--|
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |



## Application Waveforms

6) 6 6 / 54 6 &amp;37 K UNLESS OTHERWISE NOTED

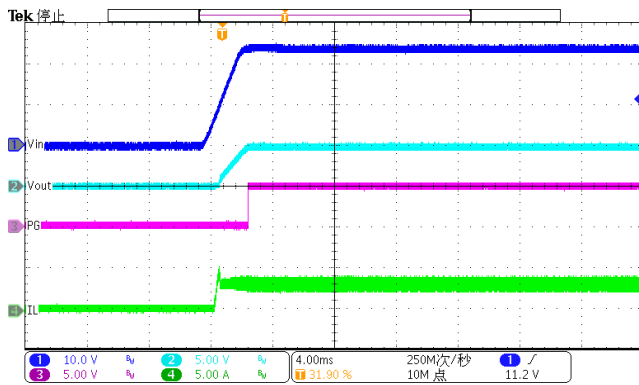


FIGURE 6 OVERUP

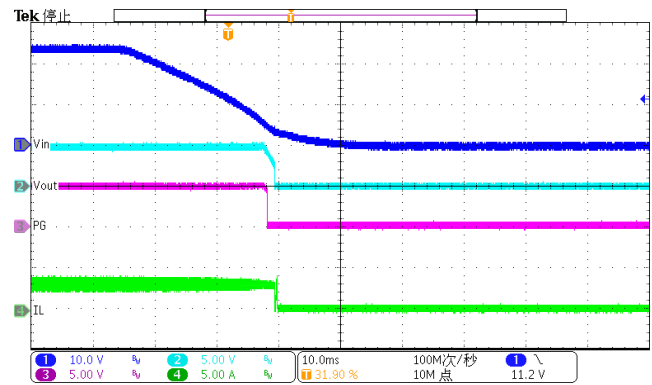


FIGURE 7 OVERDOWN

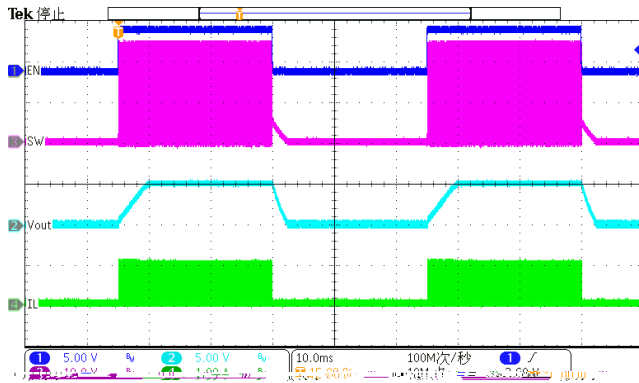


FIGURE 8 TOGGLE

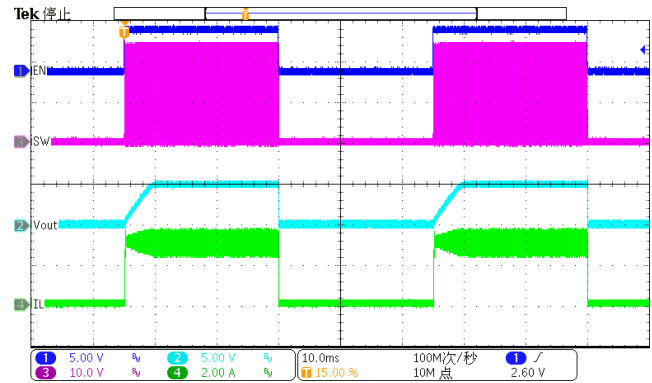


FIGURE 9 TOGGLE

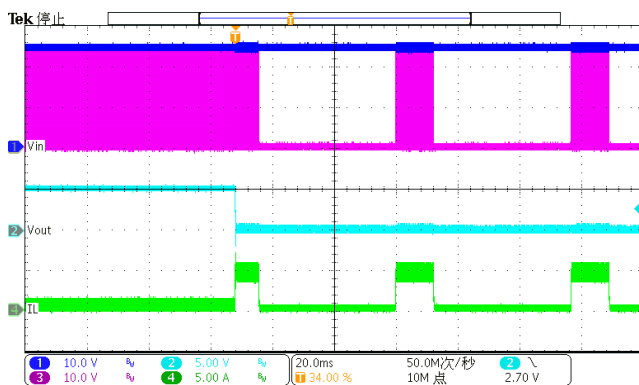


FIGURE 10 CURRENT PROTECTION TO HARD SHORT

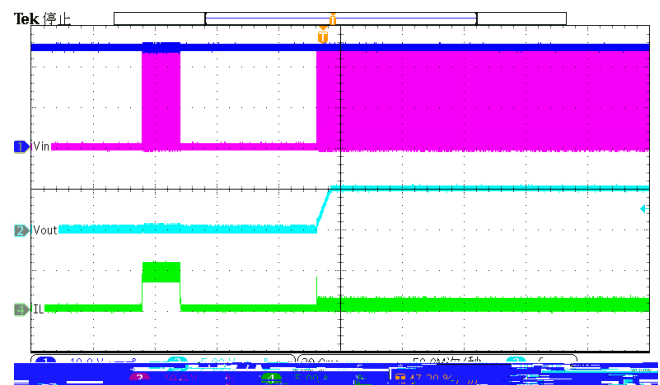


FIGURE 11 CURRENT RELEASE HARD SHORT TO

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## Application Waveforms

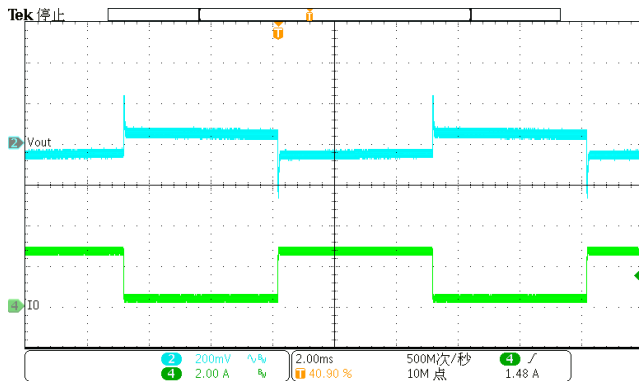


FIGURE 1, OAD 4 TRANSIENT

US

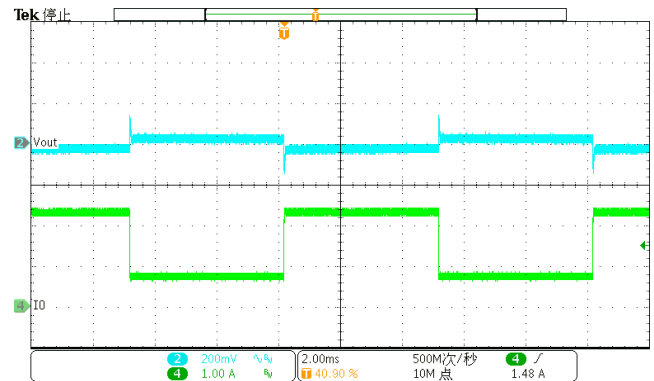


FIGURE 2, OAD 4 TRANSIENT

US

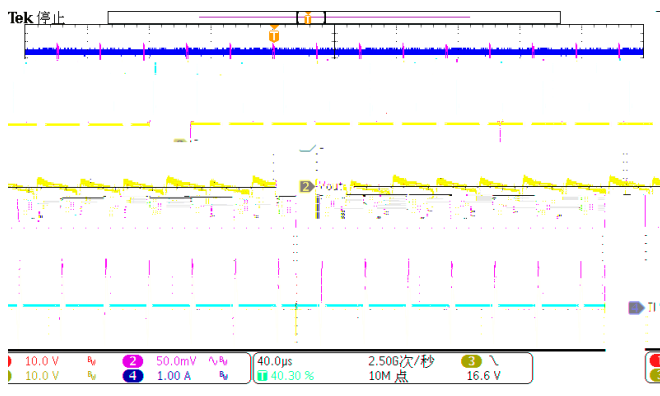


FIGURE 3, UPUT2 IPPIE

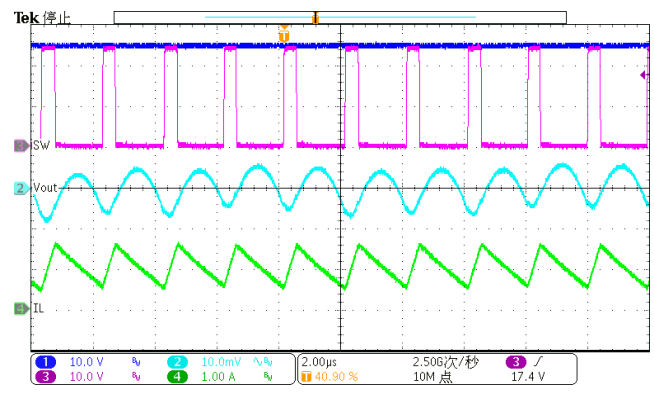


FIGURE 4, UPUT2 IPPIE

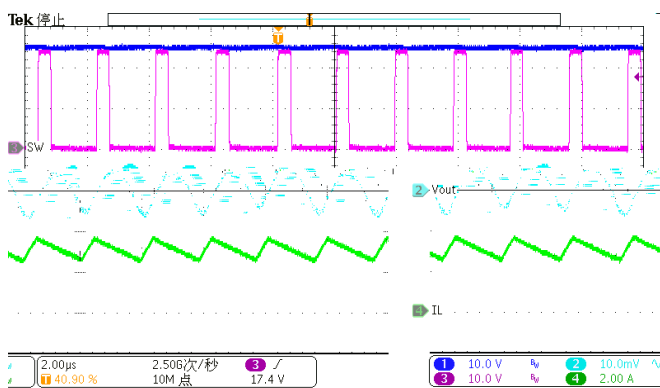


FIGURE 5, UPUT2 IPPIE



FIGURE 6, THERMAL

## Layout Guideline

0 FOPER0 LAYOUT IS A CRITICAL FOR 3 4 5 S STABLE AND EFFICIENT OPERATION 4 THE TRACES CONDUCTING FAST SWITCHING CURRENTS OR VOLTAGES ARE EASY TO INTERACT WITH STRAY INDUCTANCE AND PARASITIC CAPACITANCE TO GENERATE NOISE AND DEGRADE PERFORMANCE & OR BETTER RESULTS FOLLOW THESE GUIDELINES AS BELOW

1. 0 OVER GROUNDING SCHEME IS VERY CRITICAL BECAUSE OF CARRYING POWER THERMAL AND GLITCH BOUNCING NOISE ASSOCIATED WITH CLOCK FREQUENCY 4 THE THUMB OF RULE IS TO MAKE GROUND TRACE LOWEST IMPEDENCE AND POWER ARE DISTRIBUTED EVENLY ON 0 3 SUFFICIENTLY PLACING GROUND AREA WILL OPTIMIZE THERMAL AND NOT CAUSING OVER-HEAT AREA
2. 0 PLACE A LOW % 2 CERAMIC CAPACITOR AS CLOSE TO 6 ). PIN AND THE GROUND AS POSSIBLE TO REDUCE PARASITIC EFFECT
3. & OR OPERATION AT FULL RATED LOAD THE TOP SIDE GROUND AREA MUST PROVIDE ADEQUATE HEAT DISSIPATING AREA - AKE SURE THE TOP SWITCHING LOOP WITH POWER HAVE LOWER IMPEDENCE OF GROUNDING
4. 4 THE BOTTOM LAYER IS A LARGE GROUND PLANE CONNECTED TO THE GROUND PLANE ON TOP LAYER BY VIAS 4 THE POWER PAD SHOULD BE CONNECTED TO THE BOTTOM 0 GROUND PLANE USING MULTIPLE VIAS DIRECTLY UNDER THE ) ) IT IS RECOMMENDED MILD DIAMETER DRILL HOLES OF THERMAL VIAS BUT A SMALLER VIA OFFERS LESS RISK OF SOLDER VOLUME LOSS / N APPLICATIONS WHERE SOLDER VOLUME LOSS THRU THE VIAS IS OF CONCERN PLUGGING OR THERMATING CAN BE USED TO ACHIEVE A REPEATABLE PROCESS
5. / UPUT INDUCTOR SHOULD BE PLACED CLOSE TO THE 37 PIN 4 THE SWITCHING AREA OF THE 0 CONDUCTOR MINIMIZED TO PREVENT EXCESSIVE CAPACITIVE COUPLING
6. 4 THE 24 TERMINAL IS SENSITIVE TO NOISE SO THE 24 RESISTOR SHOULD BE LOCATED AS CLOSE AS POSSIBLE TO THE ) AND ROUTED WITH MINIMAL LENGTHS OF TRACE
7. 56, / ADJUST AND 24 RESISTORS 33 AND FEEDBACK COMPONENTS SHOULD CONNECT TO SMALL SIGNAL GROUND WHICH MUST RETURN TO THE . PIN WITHOUT ANY INTEREAVING WITH POWER GROUND
8. & OR ACHIEVING BETTER THERMAL PERFORMANCE A FOUR LAYER LAYOUT IS STRONGLY RECOMMENDED

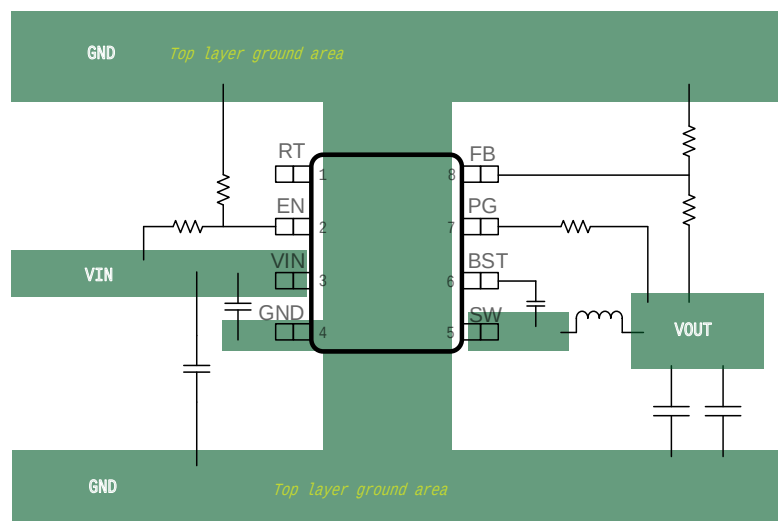


FIGURE 0 , AYCUT%AMPIE

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