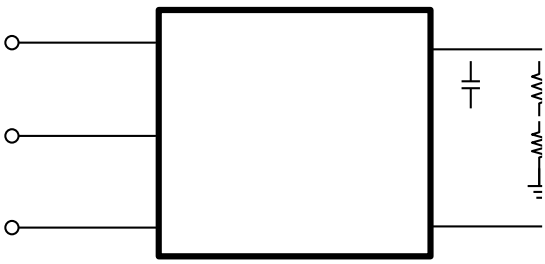


PARAMETER			UNIT
(1)			
(2)			
R JA_EVM(3)			

(1)

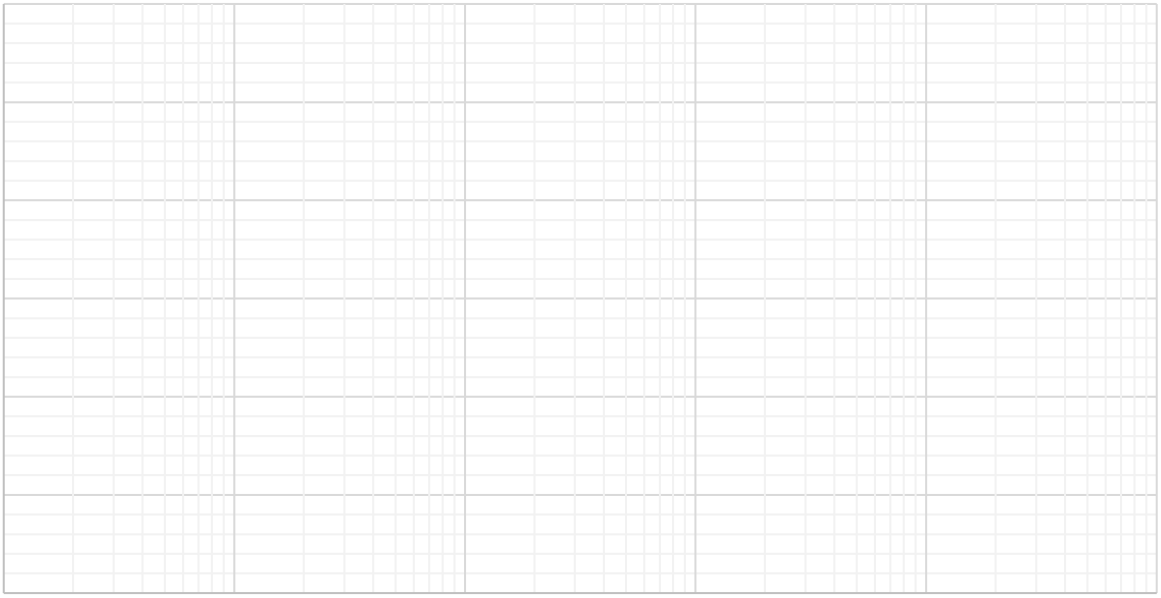
(2)

(3)

		V_{OUT}=0.8x$V_{OUT(NOM)}$,PG sink 100uA	76	
		= VPG_LOW /0.1mA		

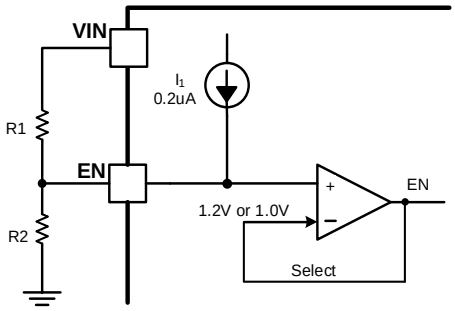
(1)
(2)
(3)
(4)

C H I

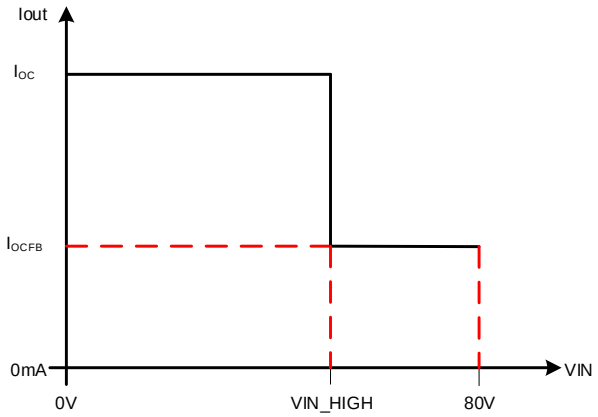


2

2



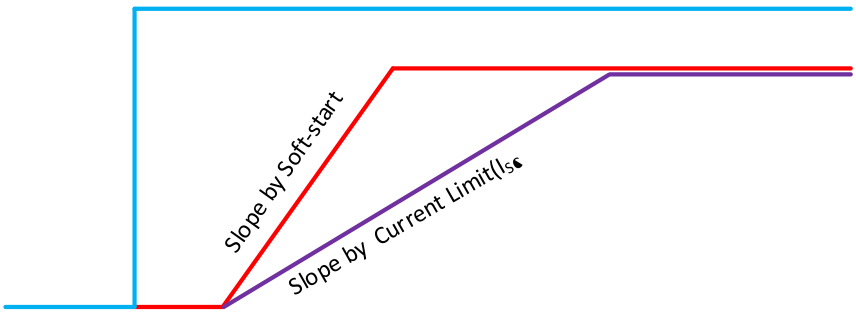
VIN_HIGH Control



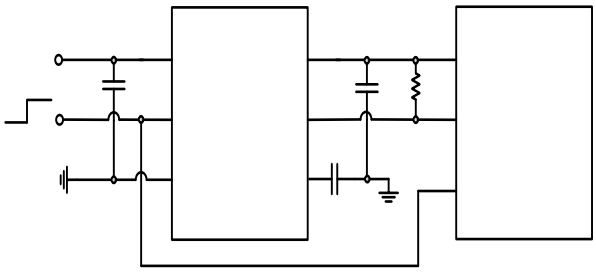
VIN_HIGH

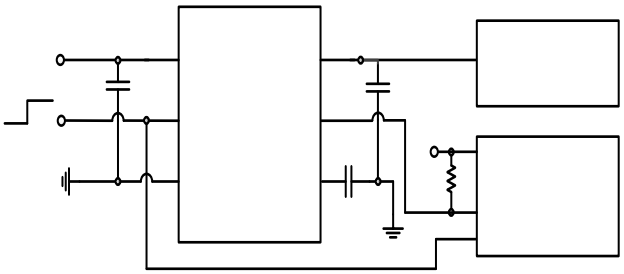
VIN_HIGH

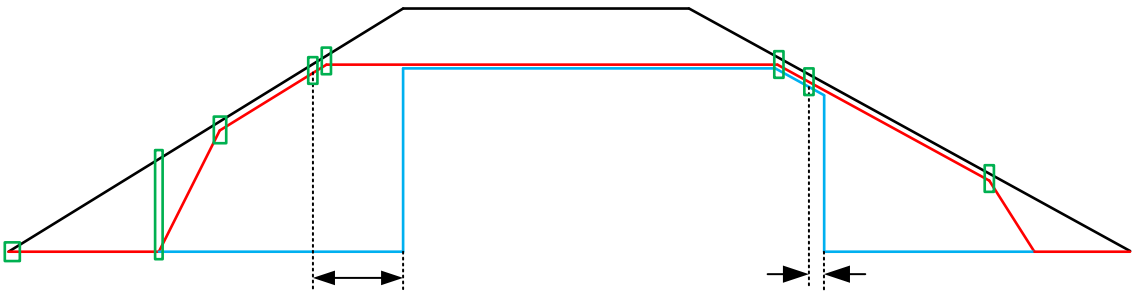
t s

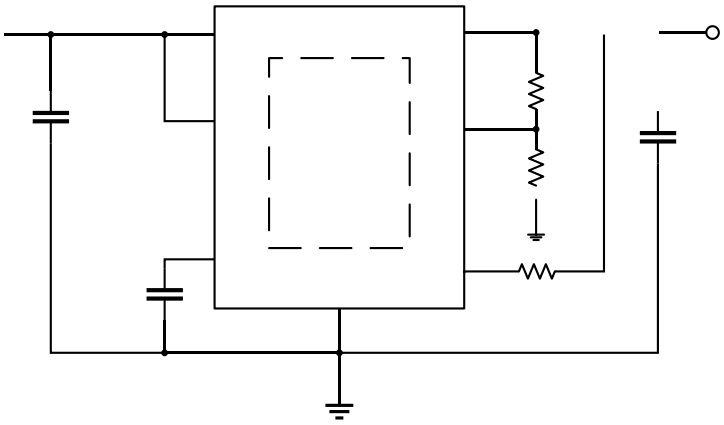


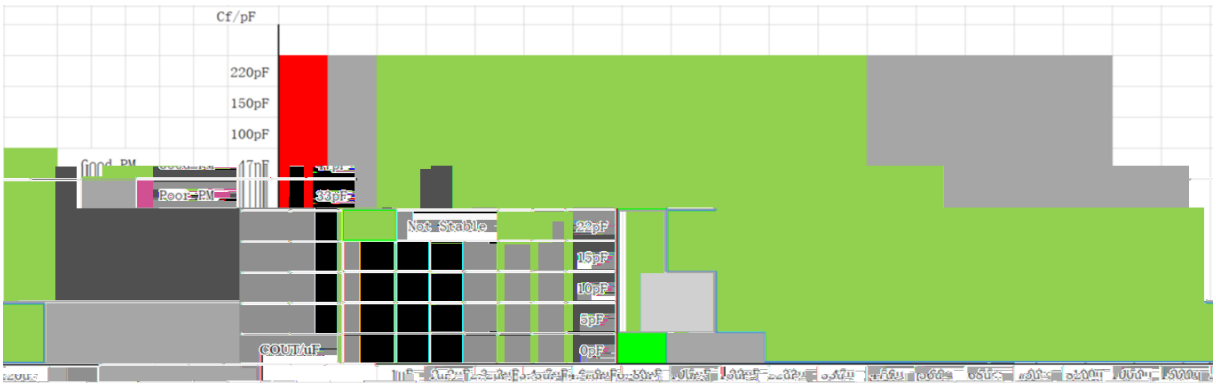
When C_{DELAY} is used, the PG output is high-impedance when V_{OUT} exceeds V_{IT}, and V_{DELAY} exceeds V_{REF}. The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF})/I_{DELAY}$. For example, when C_{DELAY}= 10 nF, the PG delay time is approximately 12 ms; that is, (10 nF × 1.2V) / 1 µA = 12 ms.

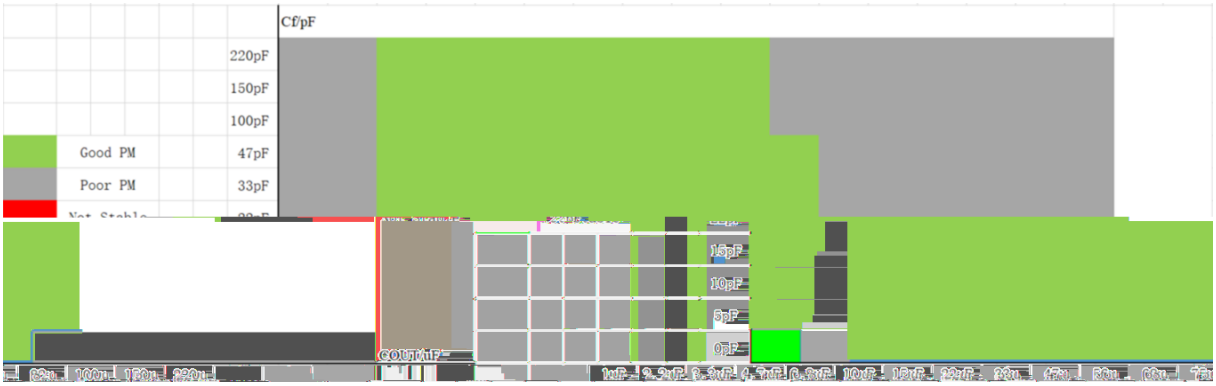


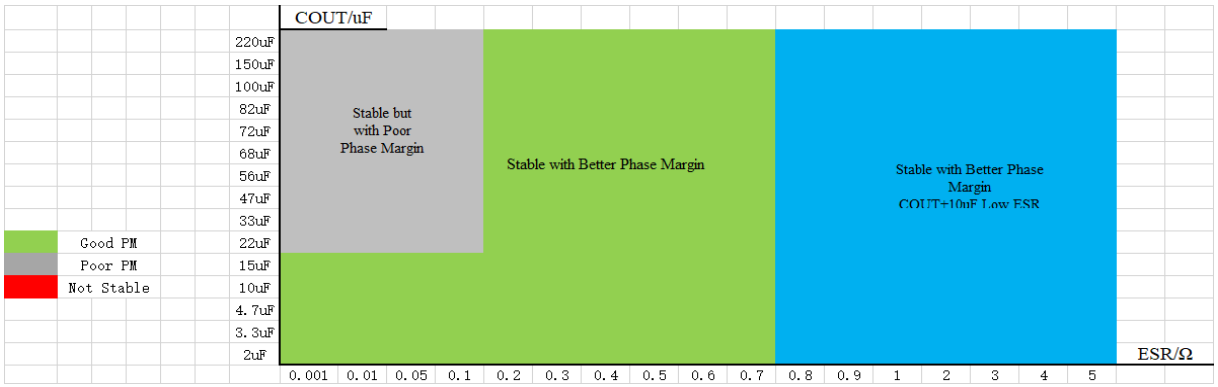




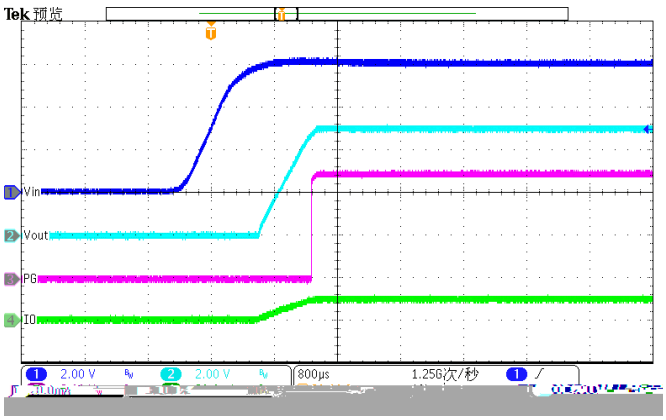


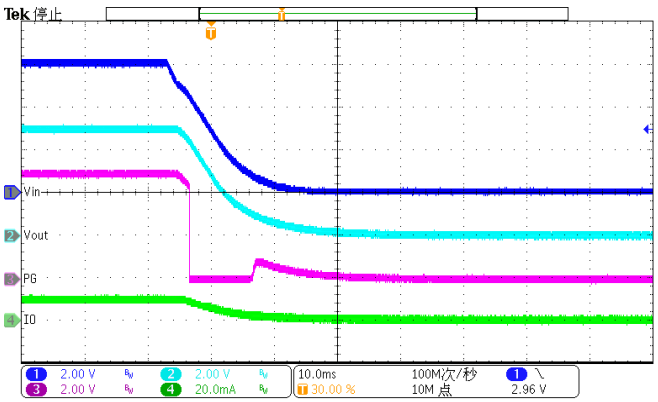

Cf/pF
220pF
150pF
100pF
47pF
33pF
Poor PM
Not Stable
22pF
15pF
10pF
5pF
0pF
COUT/uF

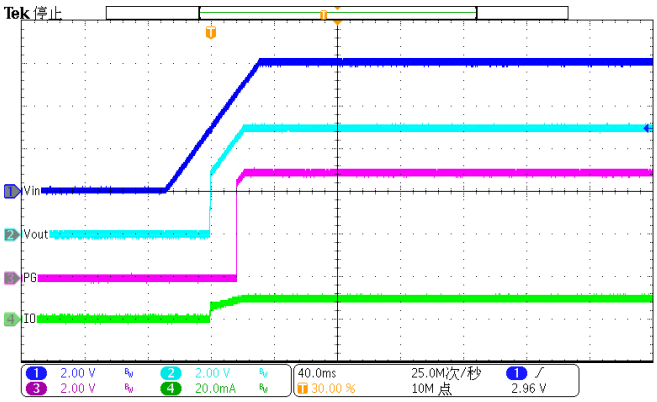

Cf/pF
220pF
150pF
100pF
Good PM
47pF
Poor PM
33pF
15pF
10pF
5pF
0pF
COUT/uF

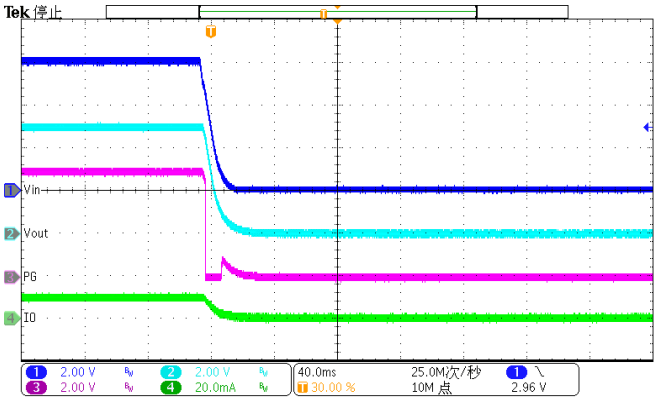

COUT/uF
220uF
150uF
100uF
82uF
72uF
68uF
56uF
47uF
33uF
22uF
15uF
10uF
4.7uF
3.3uF
2uF
Good PM
Poor PM
Not Stable
Stable but with Poor Phase Margin
Stable with Better Phase Margin
Stable with Better Phase Margin
COUT+10uF Low ESR
ESR/Ω
0.001
0.01
0.05
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
2
3
4
5

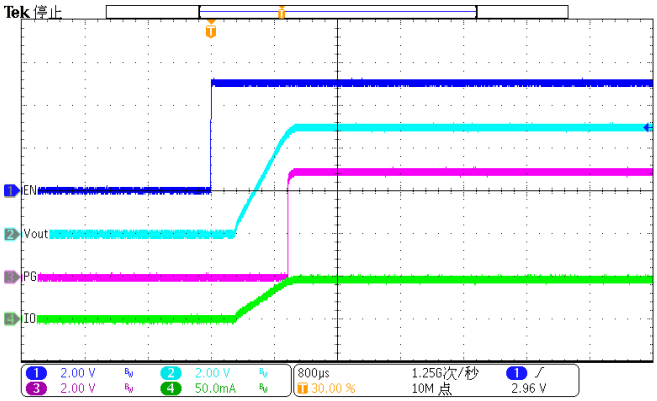
			℃

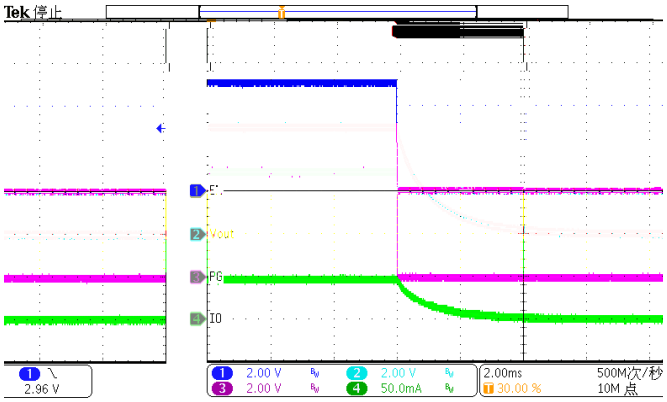

Tek 预览
Vin
Vout
PG
IO
800µs
1.25G次/秒

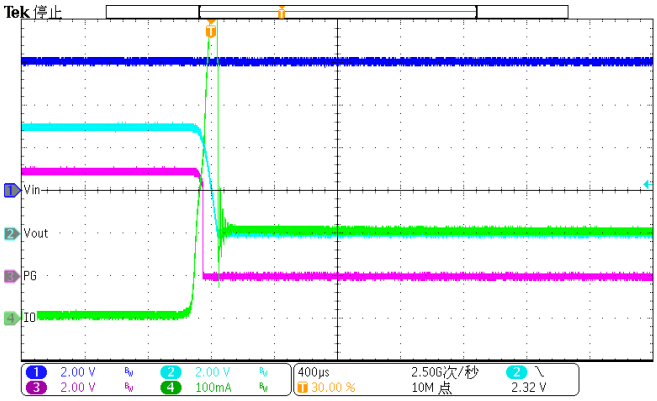

Tek 停止
Vin
Vout
PG
IO
10.0ms
100M次/秒
10M 点
2.96 V

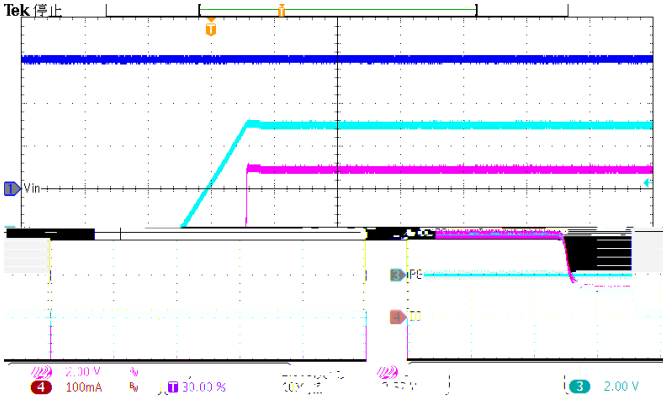

Tek 停止
Vin
Vout
PG
IO
40.0ms
25.0M次/秒
10M 点
2.96 V

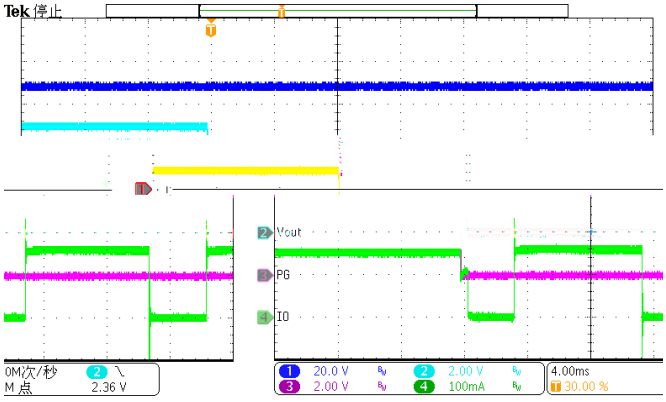

Tek 停止
Vin
Vout
PG
IO
40.0ms
25.0M次/秒
10M 点
2.96 V

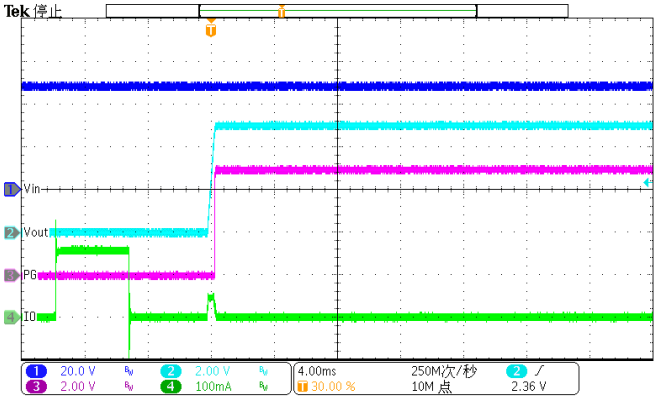

Tek 停止
EN
Vout
PG
IO
2.00 V
2.00 V
2.00 V
50.0mA
800µs
30.00 %
1.25G次/秒
10M 点
2.96 V


Tek 停止
Vout
PG
IO
2.96 V
2.00 V
2.00 V
50.0mA
2.00ms
30.00 %
500M次/秒
10M 点


Tek 停止
Vin
Vout
PG
IO
2.00 V
2.00 V
2.00 V
100mA
400µs
30.00 %
2.50G次/秒
10M 点
2.32 V


Tek 停止
Vin
PG
IO
100mA
30.00 %
2.00 V

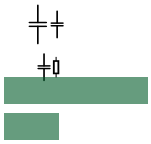

Tek 停止
Vout
PG
IO
0M次/秒
M 点
2.36 V
20.0 V
2.00 V
2.00 V
100mA
4.00ms
30.00 %

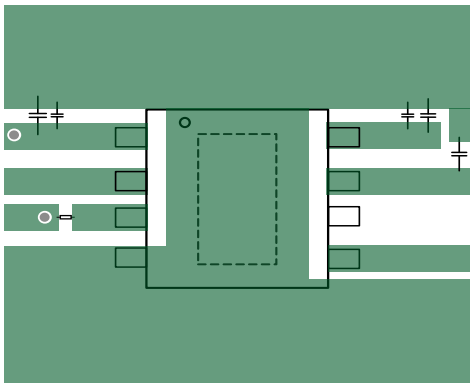

Tek 停止
Vin
Vout
PG
IO
20.0 V
2.00 V
2.00 V
100mA
4.00ms
30.00 %
250M次/秒
10M 点
2.36 V

1.
2.

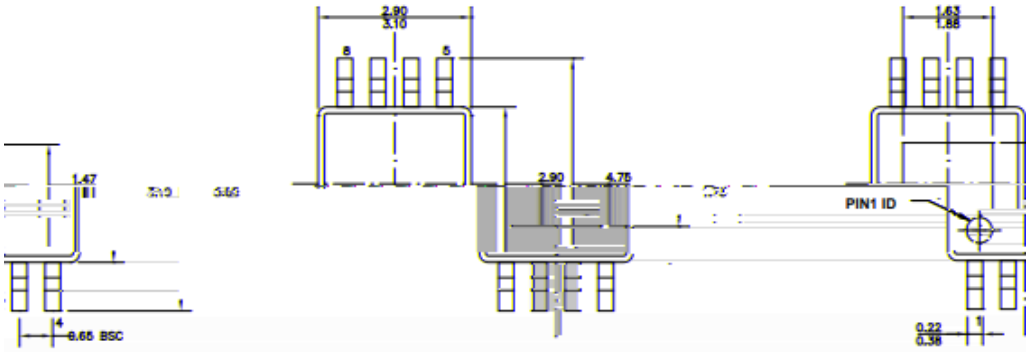
3.
4.

5.

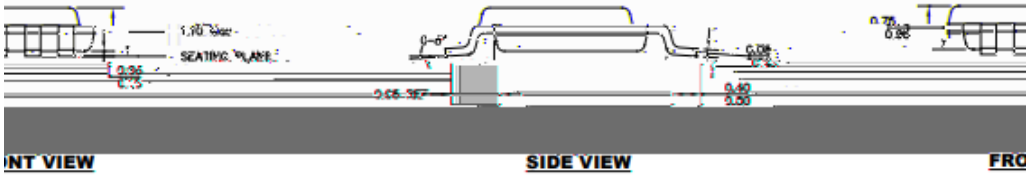




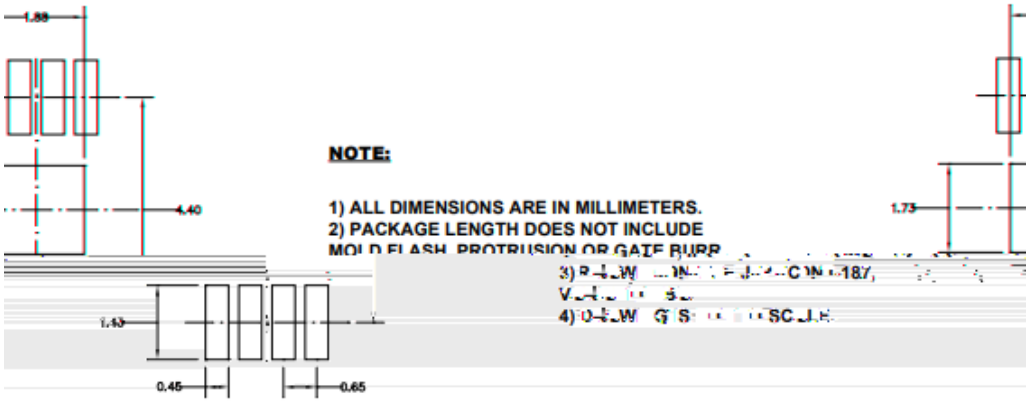
PACKAGE OUTLINE DRAWING FOR MSOP8L-EP
POD-0050 Revision 0.0



BOTTOM VIEW



SIDE VIEW



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE
MOLD FLASH, PROTRUSION OR GATE BURR
3) [illegible]
4) [illegible]

RECOMMENDED LAND PATTERN

1.
2.
3.
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5.
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