80V Input, 100mA Output Current, Low Quiescent Current LDO

x

.

Orderable Device	Output Voltage	Package	Package Marking	PINS	MSL	Transport Media, Quantity

PARAMETER	DEFINITION	MIN	MAX	UNIT

?

PARAMETER	DEFINITION	MIN	MAX	UNIT

PARAMETER	THERMAL METRIC	EMSOP-8L	UNIT
(1)			
(2)			
R JA_EVM(3)			

(1)

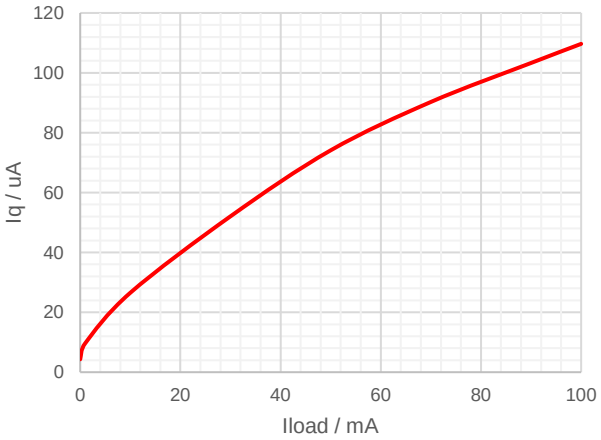
(2)

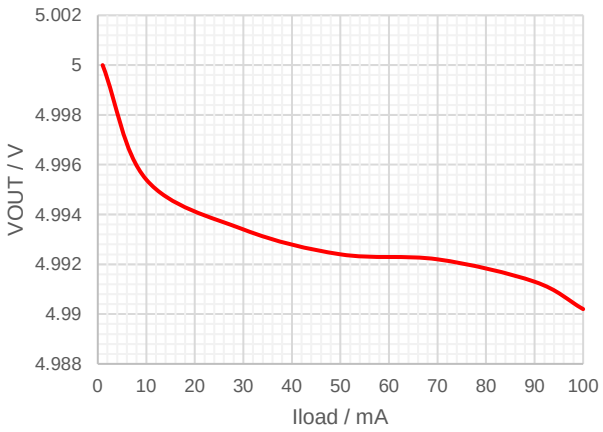
(3)

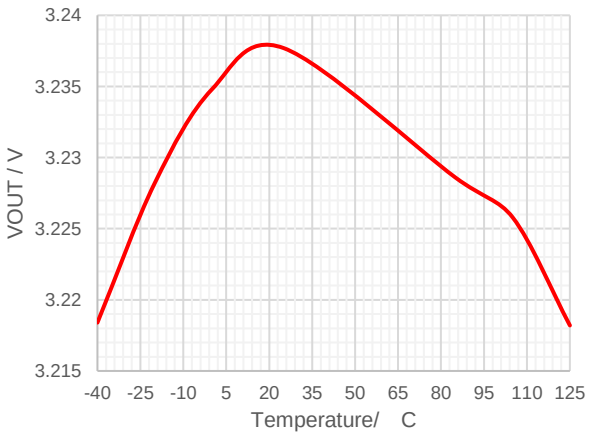
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
Regulated Output Voltage and Current						
		[redacted]				

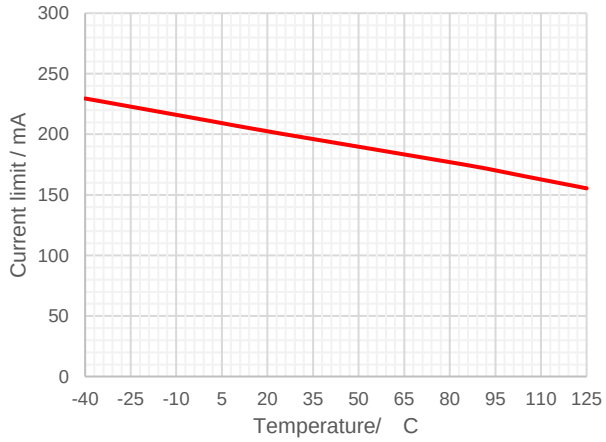
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
		= VPG_LOW /0.1mA				
Thermal Protection						

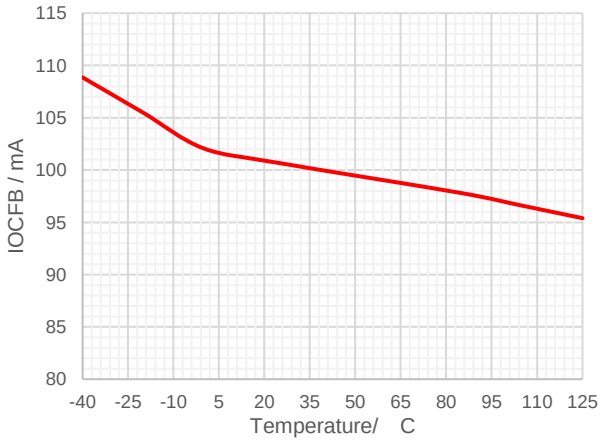
(1)
(2)
(3)
(4)

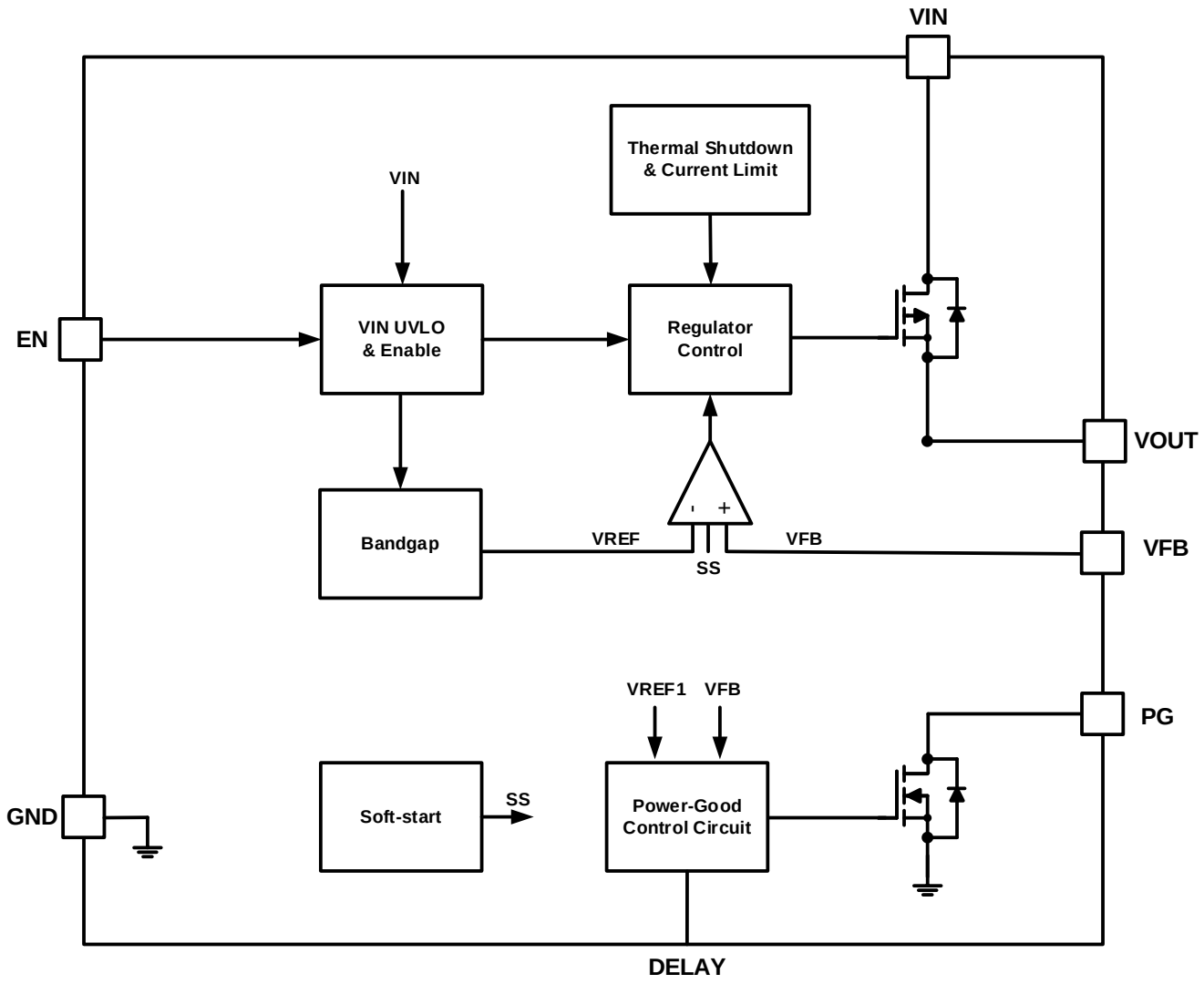

120
100
80
60
40
20
0
Iq / uA
0
20
40
60
80
100
Iload / mA


5.002
5
4.998
4.996
4.994
4.992
4.99
4.988
VOUT / V
0 10 20 30 40 50 60 70 80 90 100
Iload / mA


3.24
3.235
3.23
3.225
3.22
3.215
VOUT / V
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature/ C


300
250
200
150
100
50
0
Current limit / mA
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature/ C

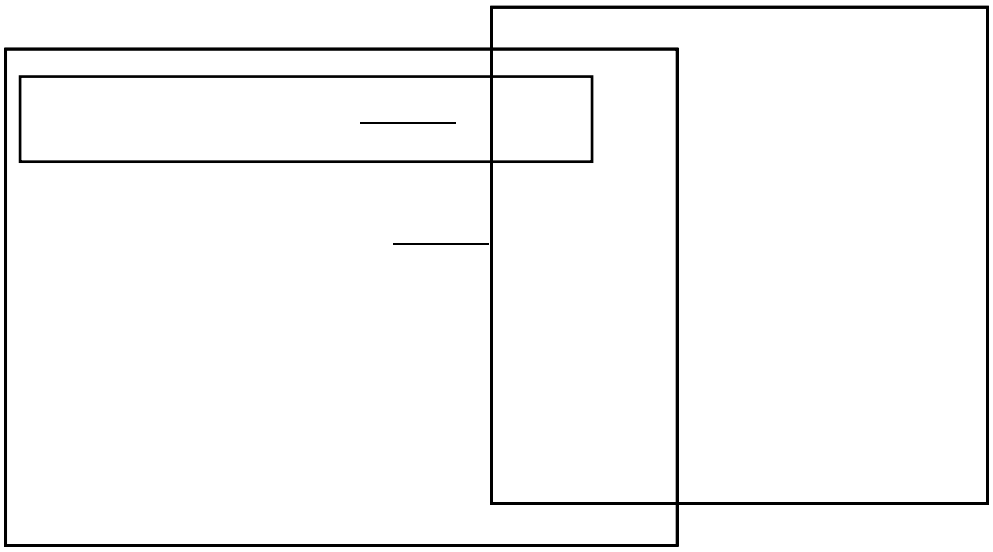

115
110
105
100
95
90
85
80
IOCFB / mA
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature/ C


VIN
Thermal Shutdown
& Current Limit
VIN
EN
VIN UVLO
& Enable
Regulator
Control
VOUT
Bandgap
VREF
SS
VFB
VFB
VREF1
VFB
PG
GND
Soft-start
SS
Power-Good
Control Circuit
DELAY

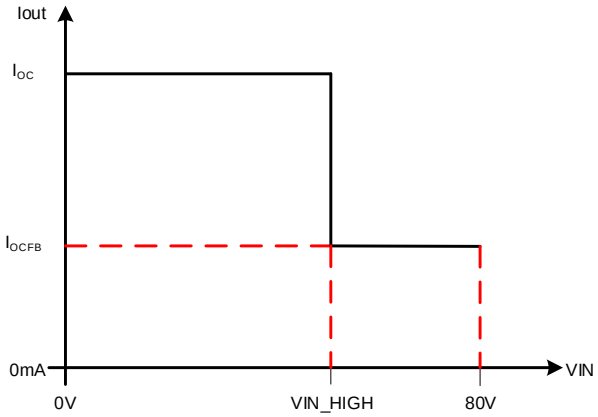
Overview

Enable and Under Voltage Lockout Threshold

U L V H



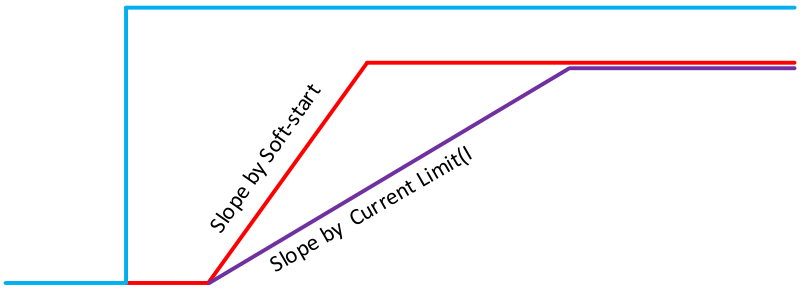
VIN_HIGH Control



Internal Soft-Start

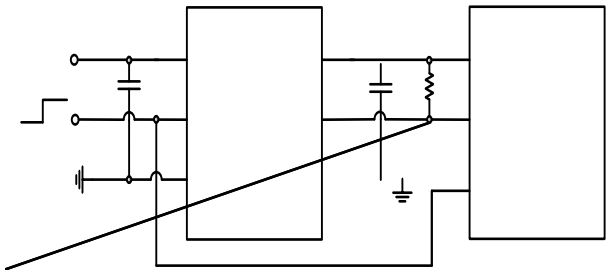
VIN_HIGH

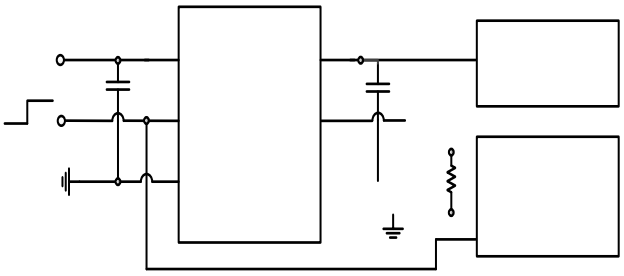
VIN_HIGH

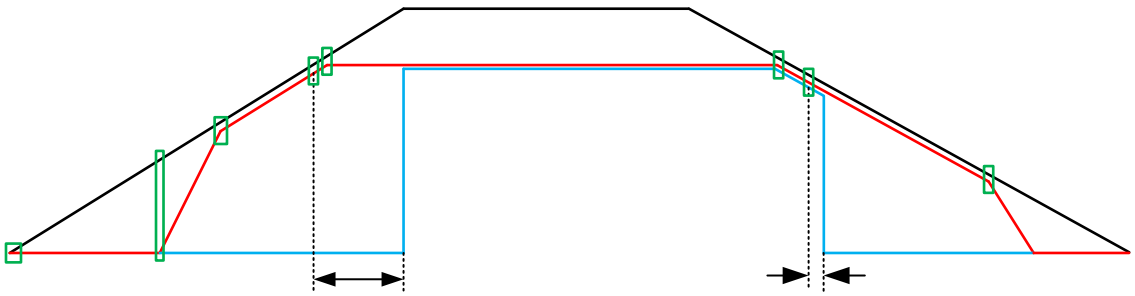


Power-Good and Power-Good Delay

When C_{DELAY} is used, the PG output is high-impedance when V_{OUT} exceeds V_{IT}, and V_{DELAY} exceeds V_{REF}. The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF})/I_{DELAY}$. For example, when C_{DELAY}= 10 nF, the PG delay time is approximately 12 ms; that is, (10 nF × 1.2V) / 1µA = 12 ms.

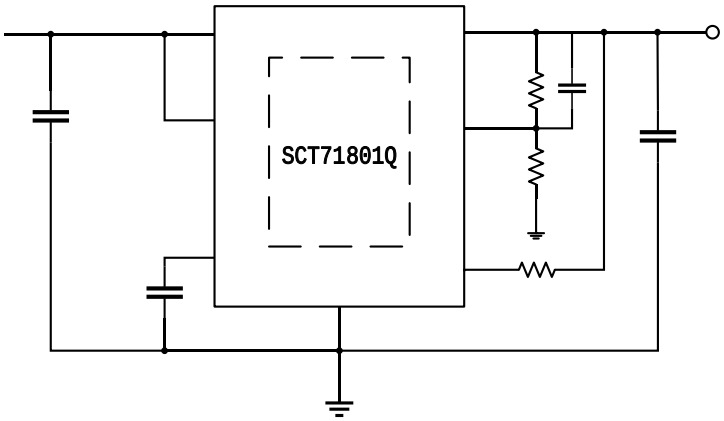






Thermal Shutdown

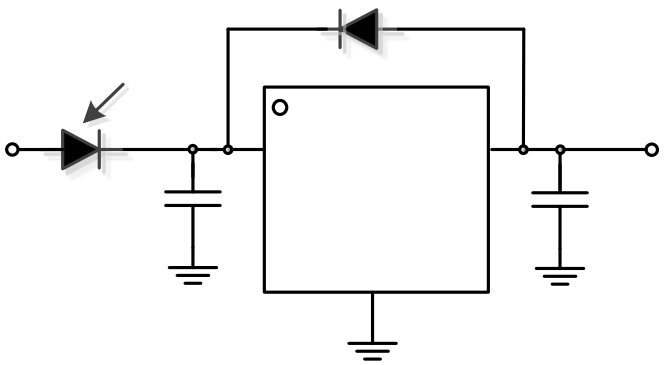
Typical application 1:



Design Parameters

Design Parameters	Example Value

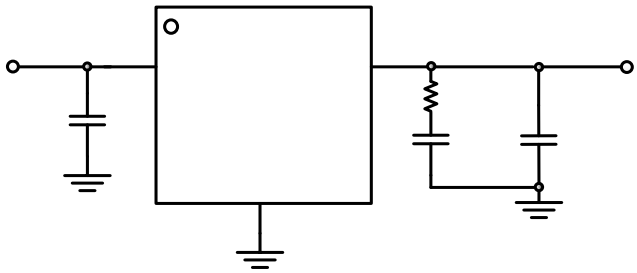
Typical application 2:



Design Parameters

Design Parameters	Example Value

Typical application 3:



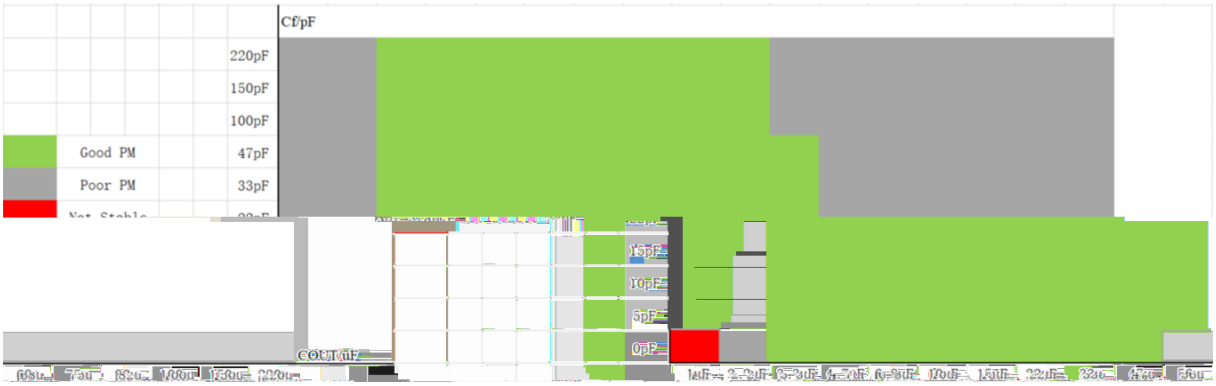
Design Parameters

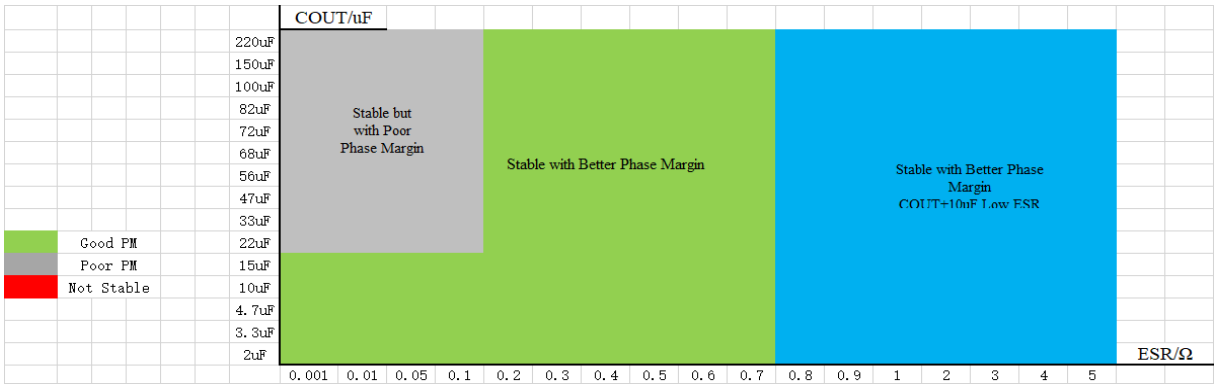
Design Parameters	Example Value

Output Voltage

Ï


Cf/pF
220pF
150pF
100pF
Poor PM
33pF
Not Stable
22pF
15pF
10pF
5pF
0pF
COUT/uF

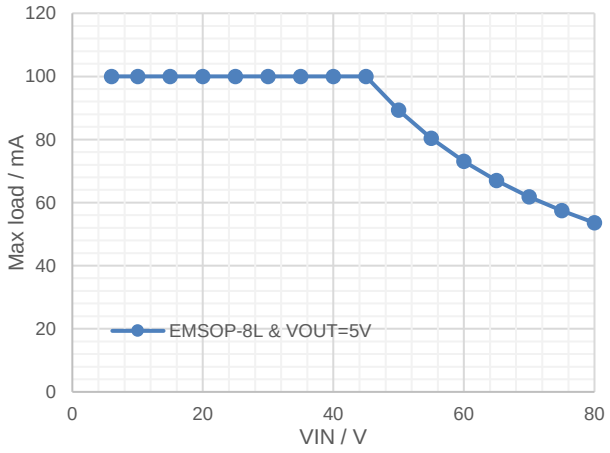

Cf/pF
220pF
150pF
100pF
Good PM
47pF
Poor PM
33pF
15pF
10pF
5pF
0pF
COUT/uF

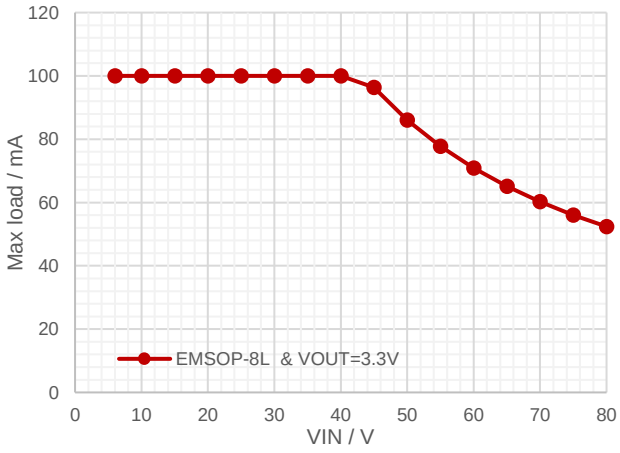

COUT/uF
220uF
150uF
100uF
82uF
72uF
68uF
56uF
47uF
33uF
22uF
15uF
10uF
4.7uF
3.3uF
2uF
Good PM
Poor PM
Not Stable
Stable but with Poor Phase Margin
Stable with Better Phase Margin
Stable with Better Phase Margin COUT+10uF Low ESR
ESR/Ω
0.001
0.01
0.05
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
2
3
4
5

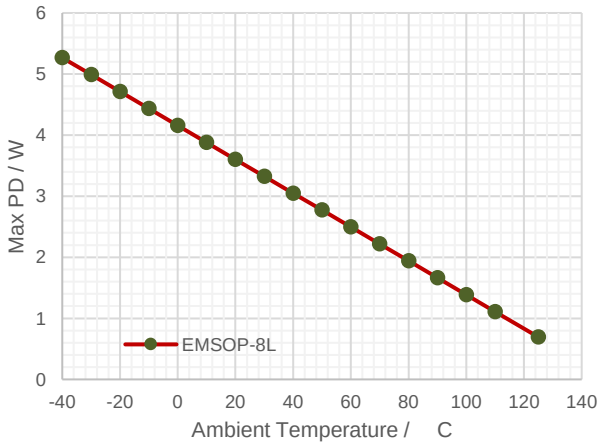
Power Dissipation and Thermal Performance

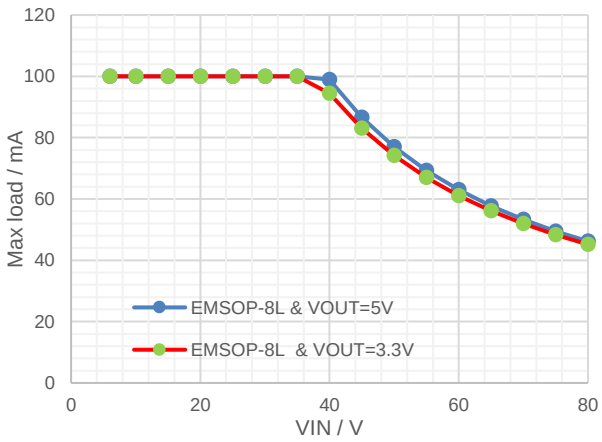
Thermal Performance of Different Packages Based on EVM Test

Package	Max Allowable PD (W) (Not Trigger TSD,VOUT=5V)	Max Allowable PD (W) (TJ≤150)	R_{JA_EVM} (℃/W)

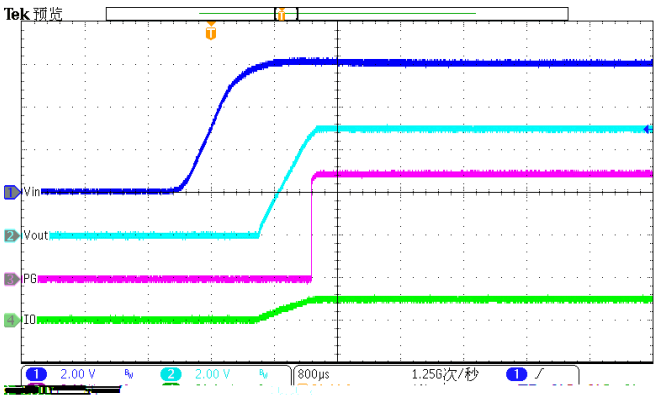

Max load / mA
VIN / V
EMSOP-8L & VOUT=5V

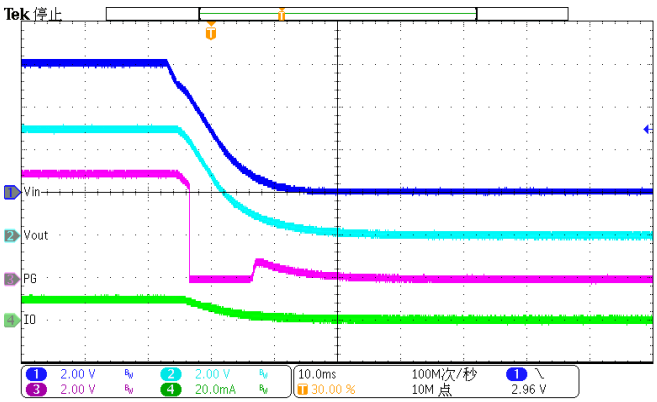

Max load / mA
VIN / V
EMSOP-8L & VOUT=3.3V

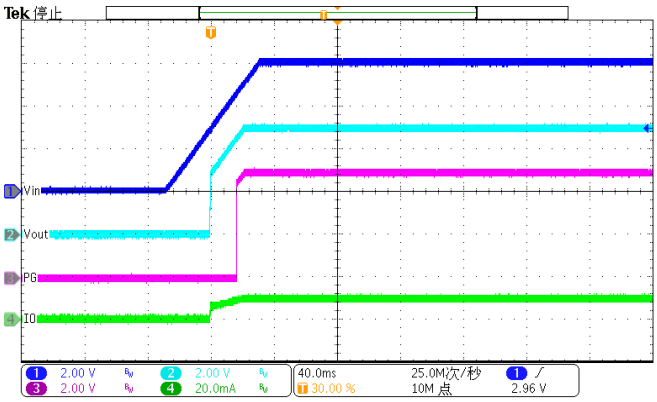

Max PD / W
Ambient Temperature / C
EMSOP-8L

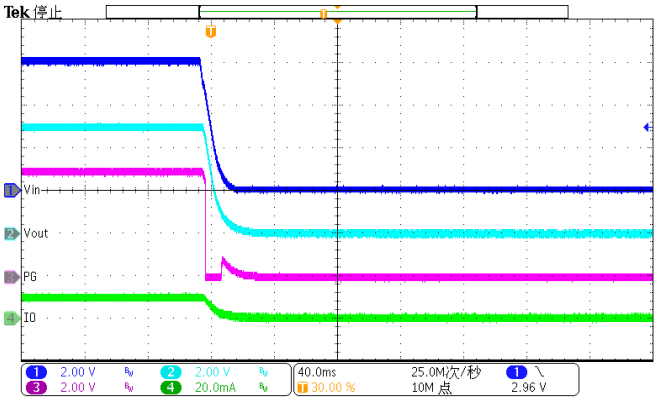

Max load / mA
VIN / V
EMSOP-8L & VOUT=5V
EMSOP-8L & VOUT=3.3V

Application Waveforms

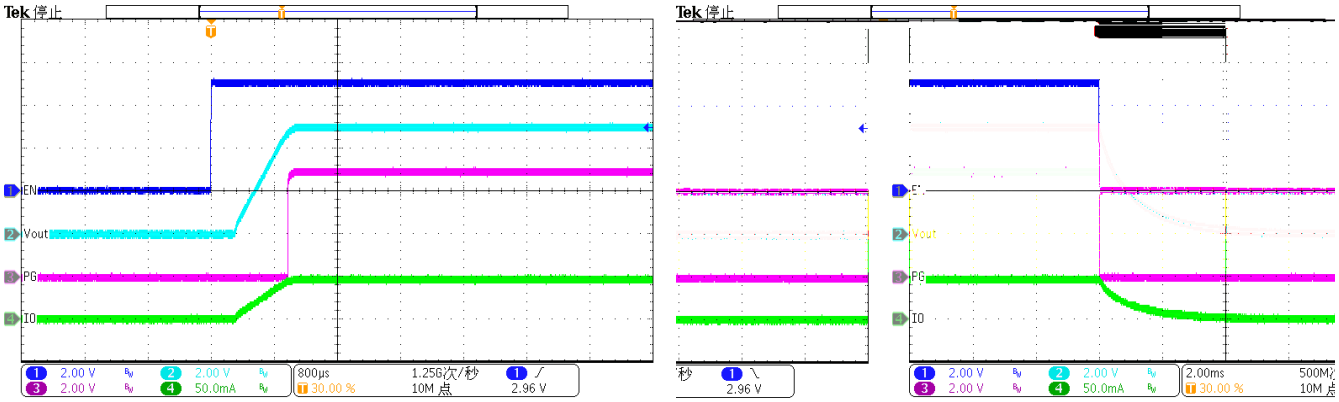


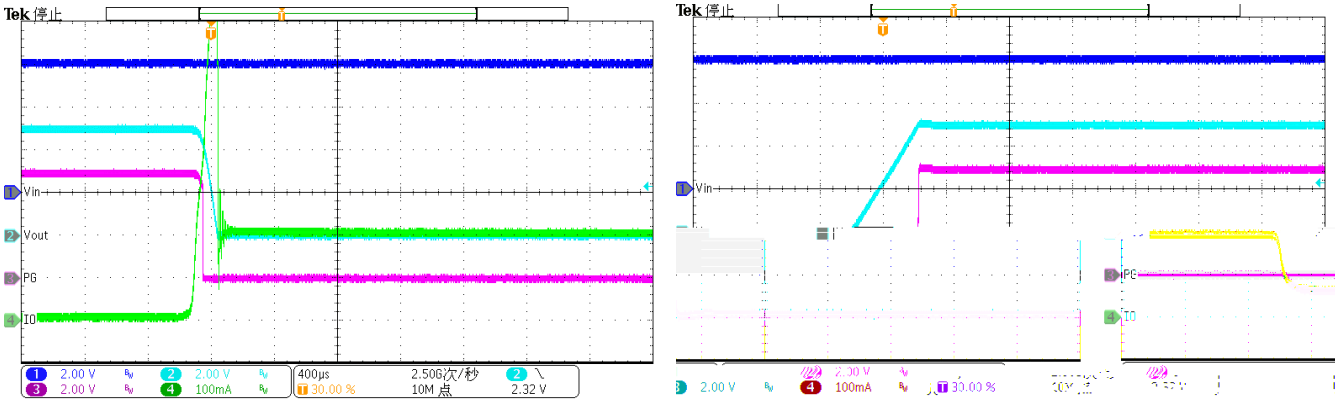


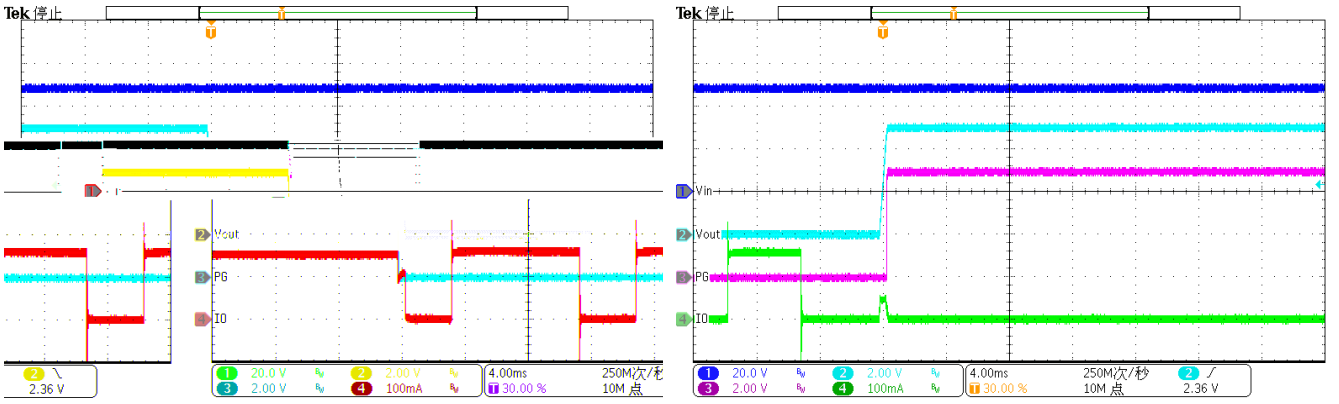




Application Waveforms(Continued)





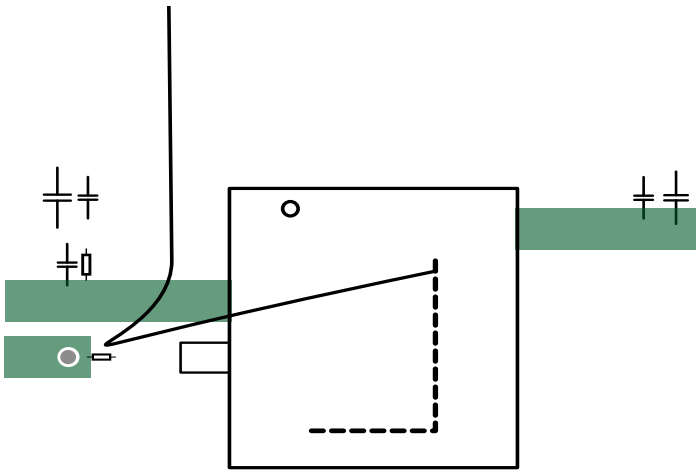


Layout Guideline

1.
2.

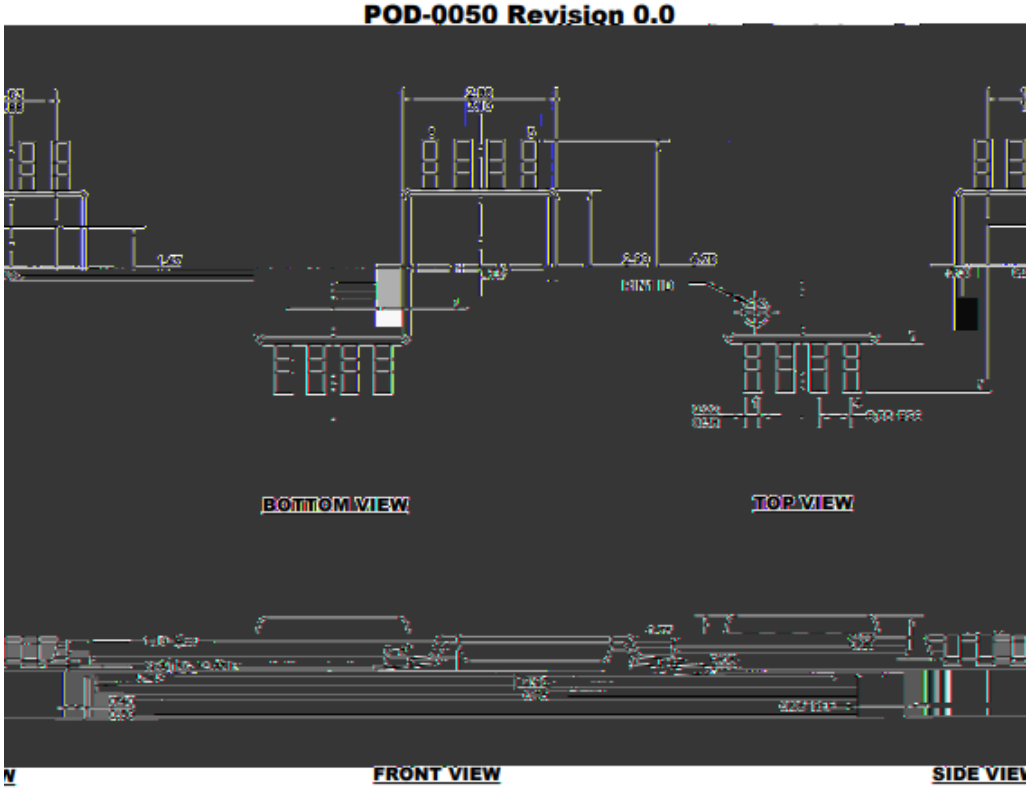
3.
4.

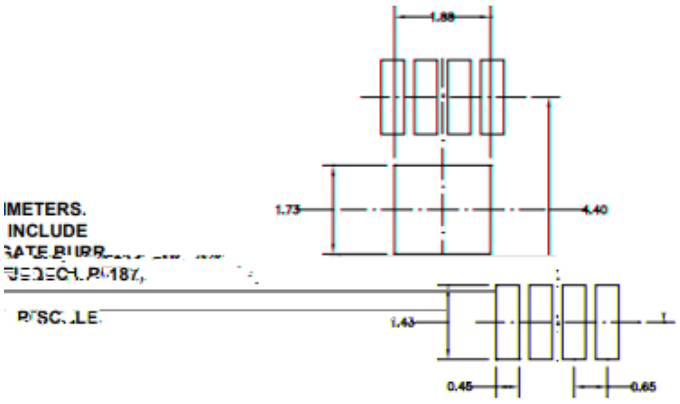
5.



SCT71801A00QMTER

PACKAGE OUTLINE DRAWING FOR MSOP8L-EP
POD-0050 Revision 0.0





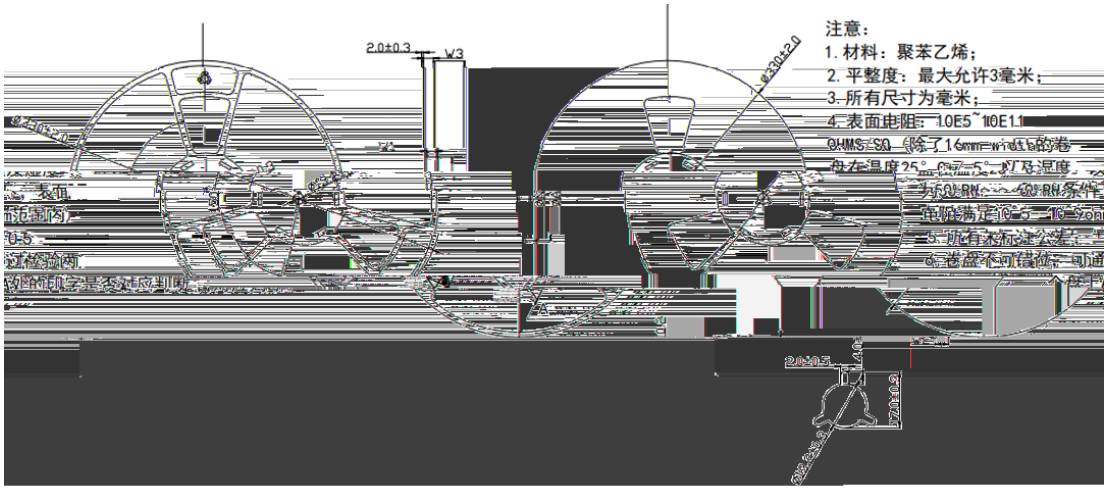
NOTE:

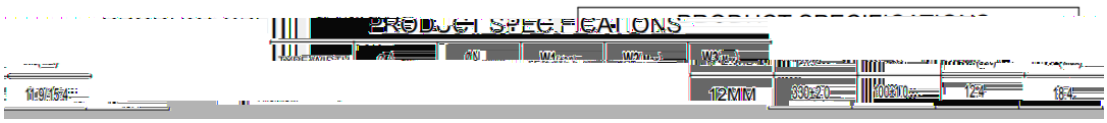
1) ALL DIMENSIONS ARE IN MILL
2) PACKAGE LENGTH DOES NOT

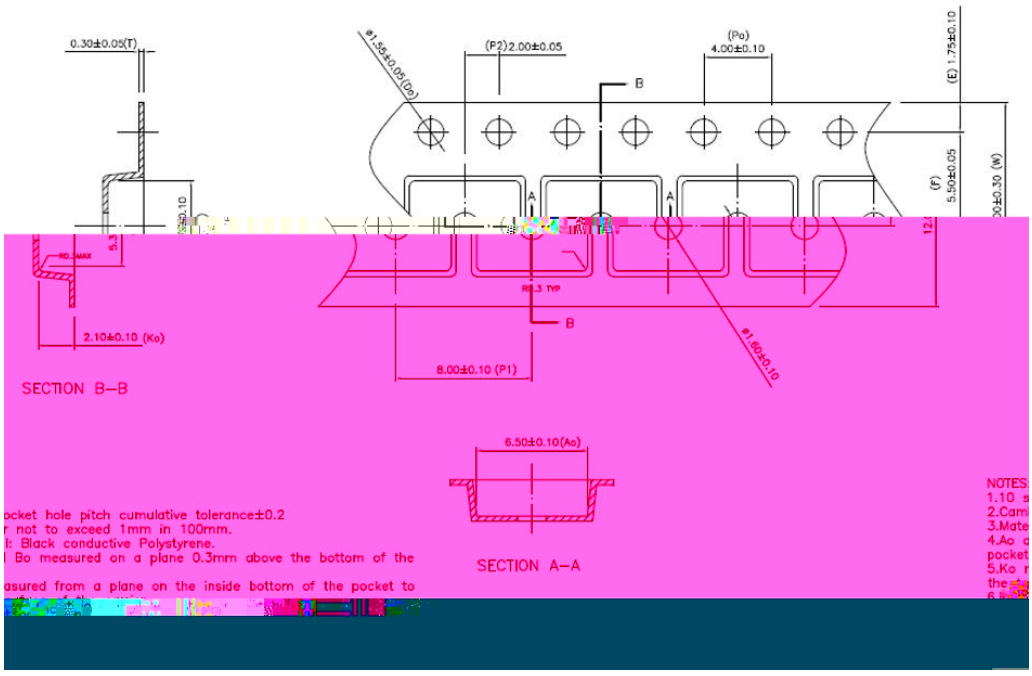
RECOMMENDED LAND PATTERN

NOTE:

1.
2.
3.
4.
5.
6.


注意：
1. 材料：聚苯乙烯；
2. 平整度：最大允许3毫米；
3. 所有尺寸为毫米；
2.0±0.3
W3
12MM




0.30±0.05(T)
(P2)2.00±0.05
(Po)
4.00±0.10
(E) 1.75±0.10
(F)
5.50±0.05
2.10±0.10 (Ko)
8.00±0.10 (P1)
SECTION B–B
6.50±0.10(Ao)
SECTION A–A
User Direction of Feed

NOTICE: