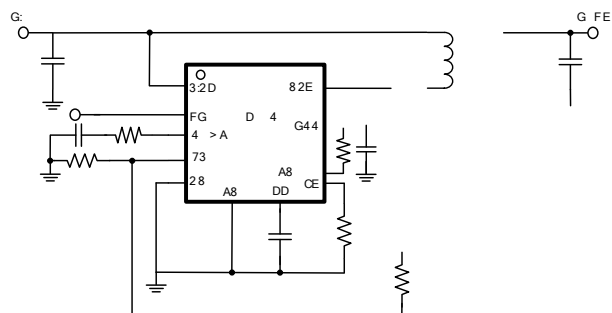
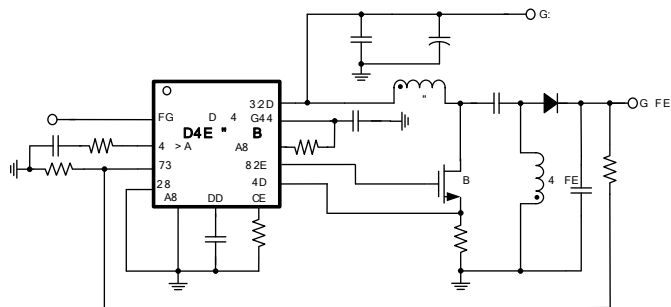
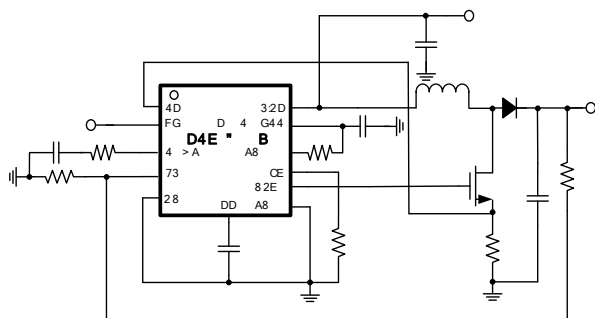




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Rev.1.2

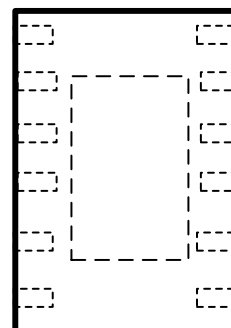


SCT81623Q



ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL

DESCRIPTION	MIN	MAX	UNIT



Top View: 12-Lead Plastic DFN 2mmx3mm

NAME	NO.	DESCRIPTION

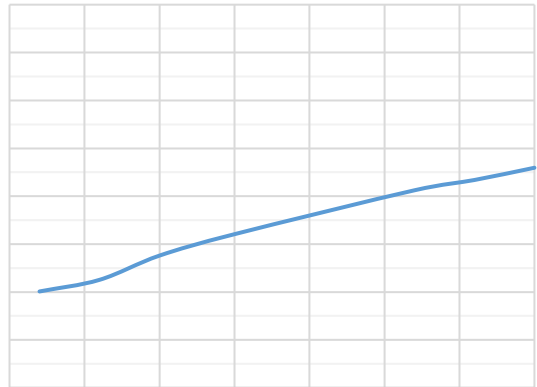
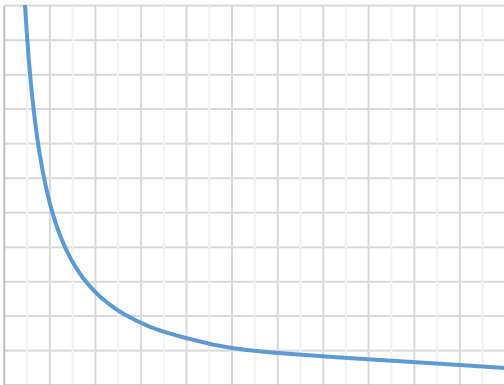
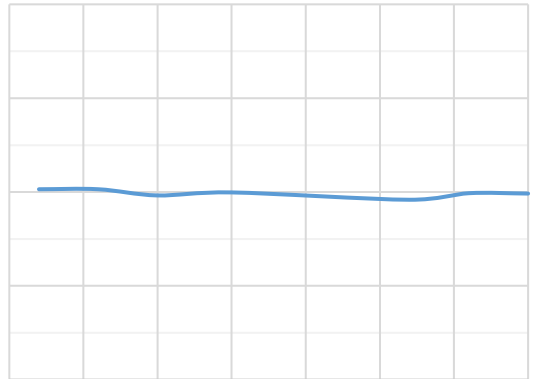
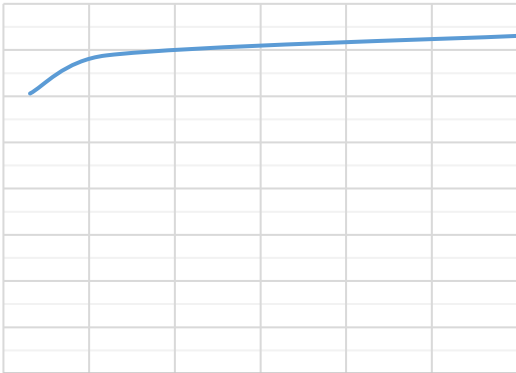
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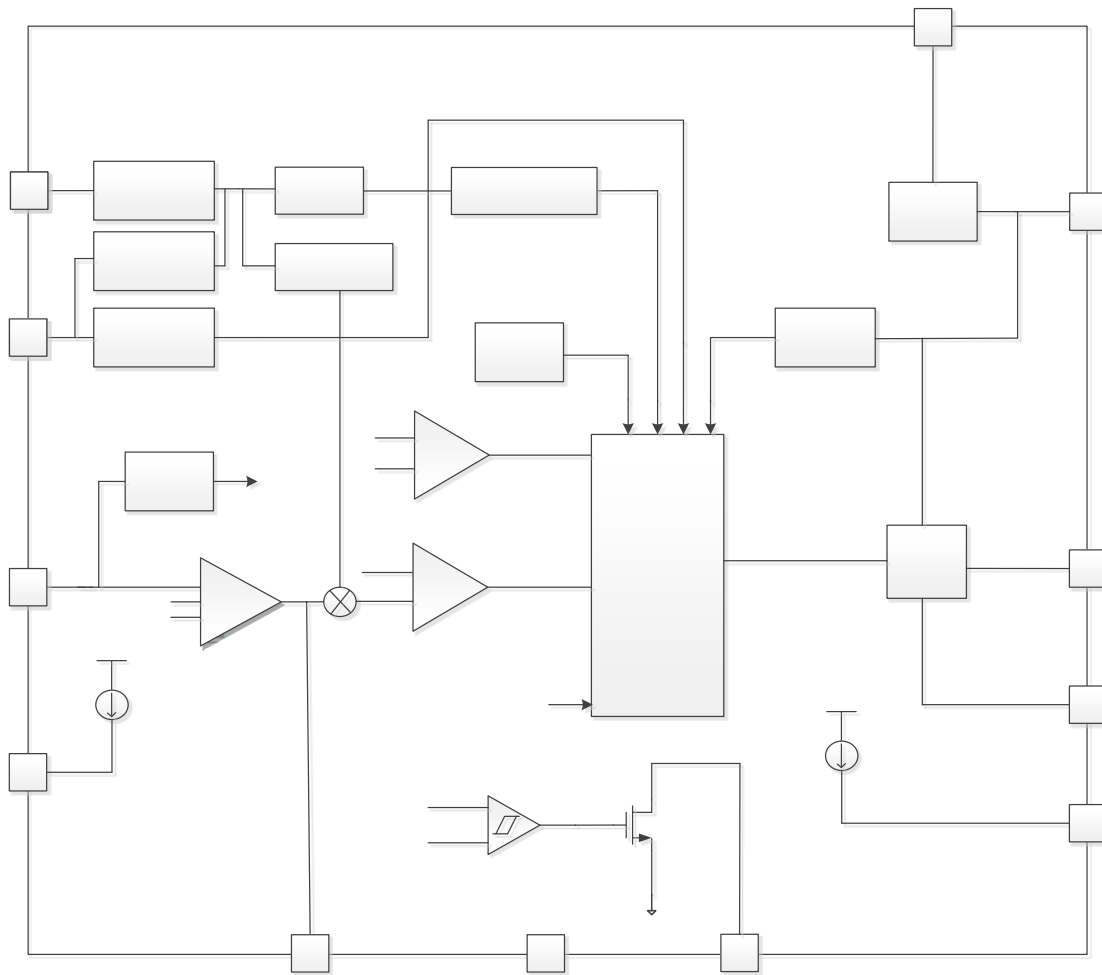
NAME	NO.	DESCRIPTION

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
VCC Power						
UVLO/EN/SYNC						
Reference and Control Loop						
Gate Driver						

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Current Sense						
Soft start						
PGOOD						
Switching Frequency						
Protection						

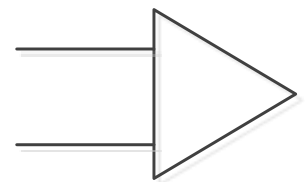
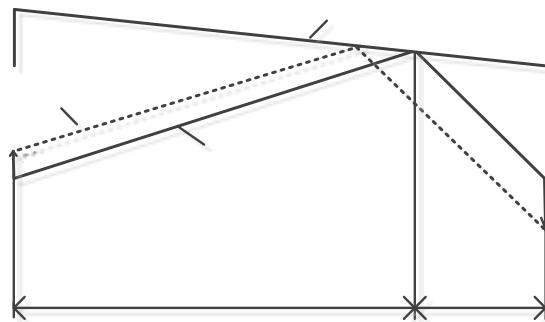




Overview

Overvoltage Protection

Slope Compensation Ramp



:

*

:

1 *

2 *

1 * * /

2 * () * /

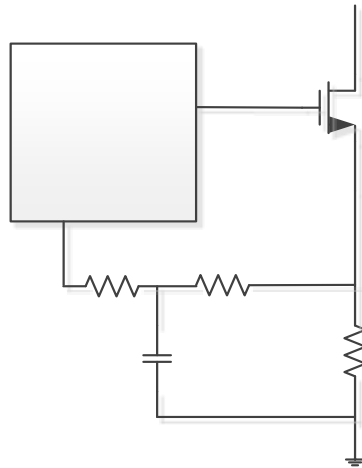
1 ($\frac{2}{1}$) * 0

1 ($\frac{2}{1}$) * 0 ($\frac{1}{1}$) * 0

$\left| \left(\frac{2}{1} \right) \right| 1$

*

(*) *

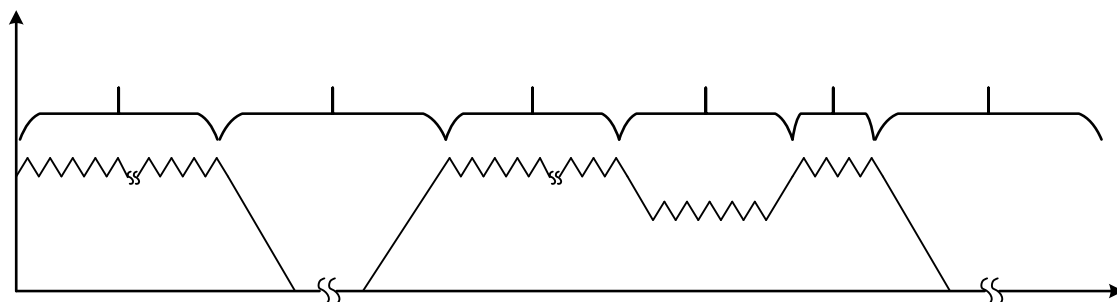


Adjustable Peak Current Limit

40

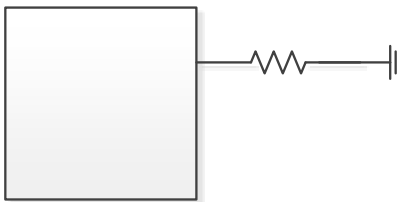
3

1



Output Voltage

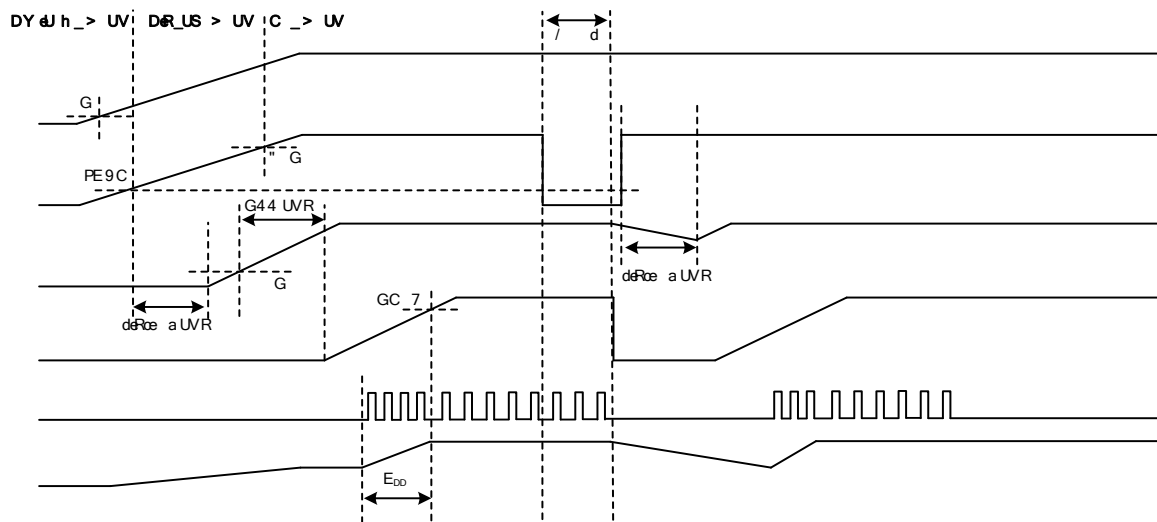
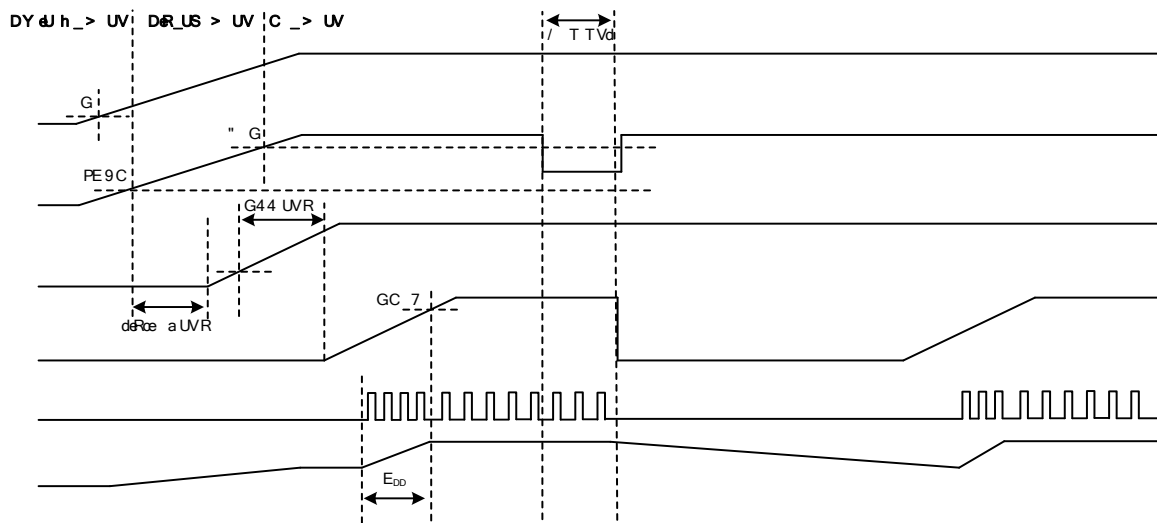
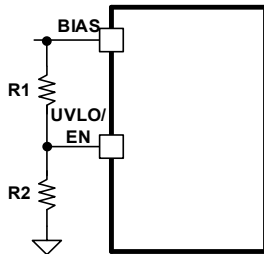
Switching Frequency



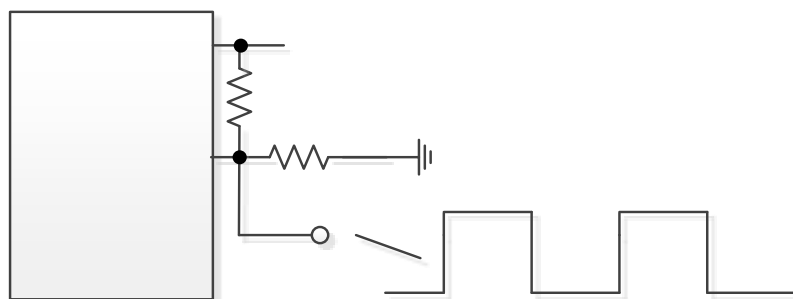
Enable and Under Voltage Lockout

1 _____

2 1* _____



Clock Synchronization



Programmable Soft-Start

—

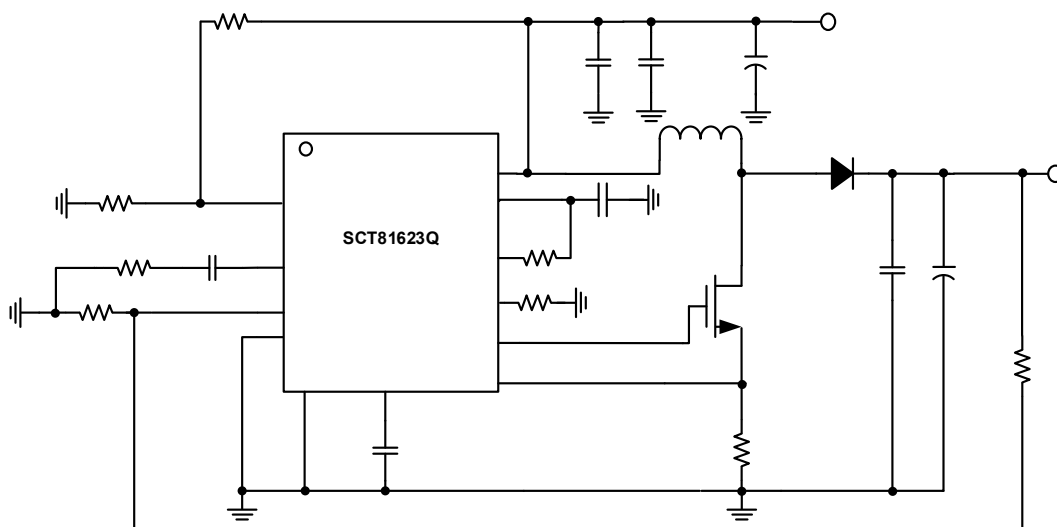
MOSFET Driver

D AA A

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Frequency Spread Spectrum

Typical Application (Boost)



Design Parameters

Design Parameters	Example Value

Inductor Selection (Boost)

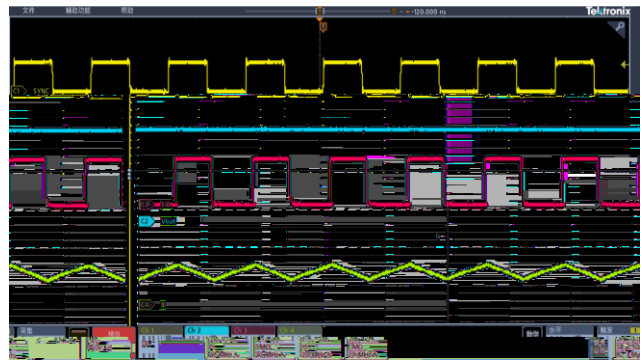
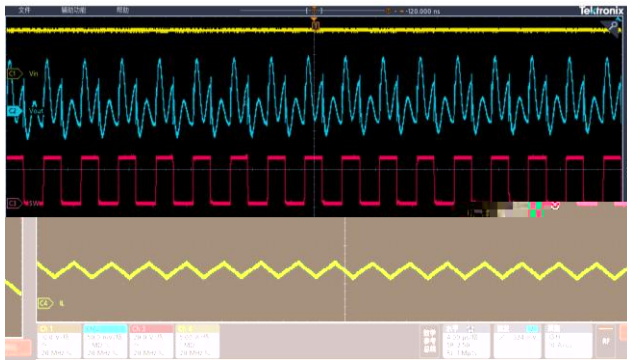
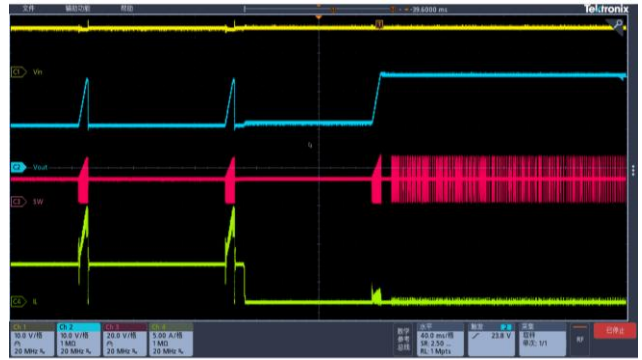
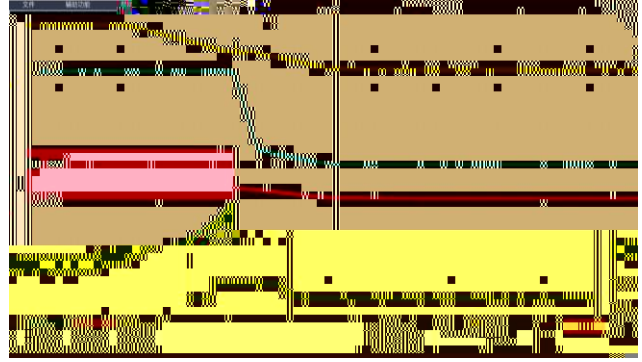
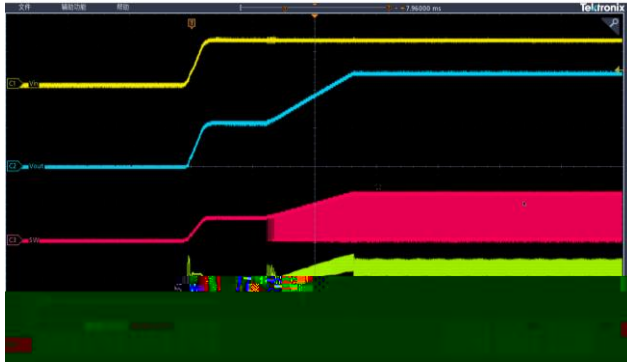
$$\frac{1}{\frac{1}{\quad} \quad \frac{1}{\quad}}$$

/

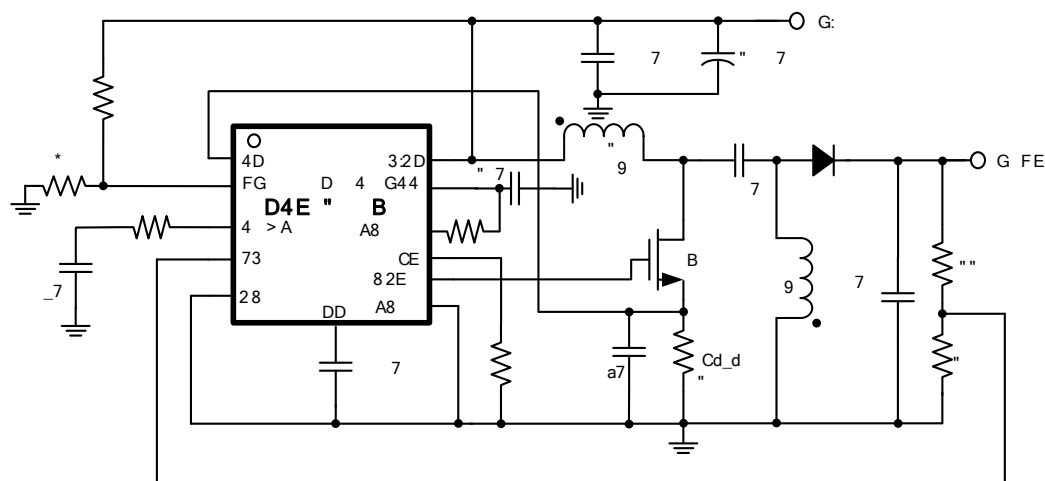
Output Diode Selection

$$\left(\quad \right) \overline{(1 \quad)}$$

Application Waveforms



Typical Application(Sepic)



Design Parameters

Design Parameters	Example Value

Inductor Selection (Sepic)

$$I_1 \quad 40\% = \frac{I_1}{I_2} \quad 40\%$$

$$I_2 \quad 40\% = \frac{I_2}{I_1} \quad 40\%$$

$$I_1 \quad I_2 = \frac{I_1}{I_2}$$

f

$$I_1 = \frac{I_1}{2} \quad \frac{I_1}{2} \quad (1 - \frac{40\%}{2})$$

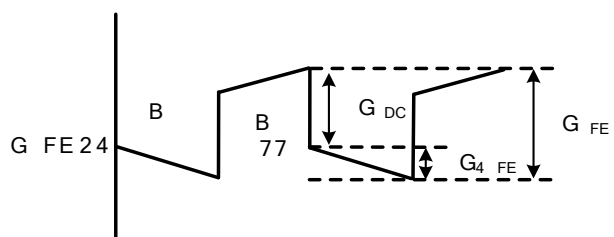
$$I_2 = \frac{I_2}{2} \quad (1 - \frac{40\%}{2})$$

$$I_1 \quad I_2 \quad \frac{I_1}{2} = \frac{I_2}{2}$$

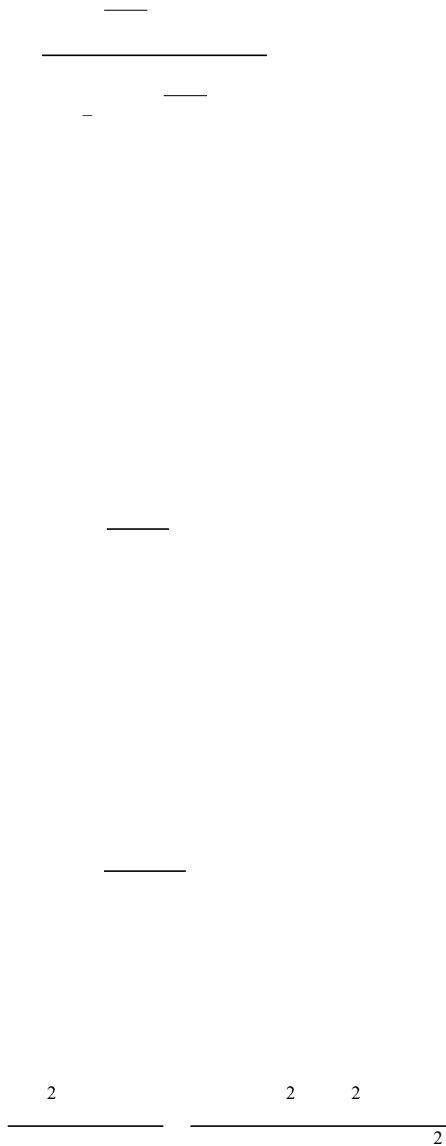
Power MOSFET Selection

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Transformer Selection (Flyback)



$$- \frac{\quad}{2} \quad \frac{\quad}{2}$$

MOSFET and Diode Selection

$$- \quad 1.5 \sim 2 \quad - \quad \frac{\quad}{\quad}$$

$$- \quad 1.2 \sim 1.5 \quad - \quad \frac{\quad}{\quad}$$

$$- \quad \sqrt{\frac{\quad^2}{\quad} + \frac{\quad^2}{12}}$$

Output Capacitor Selection

$$\frac{\quad}{5} \quad \frac{\quad^2}{2} \quad \frac{\quad^2}{5} \quad \frac{1}{2} \quad \frac{\quad^2}{\quad}$$

$$\frac{\quad}{2}$$

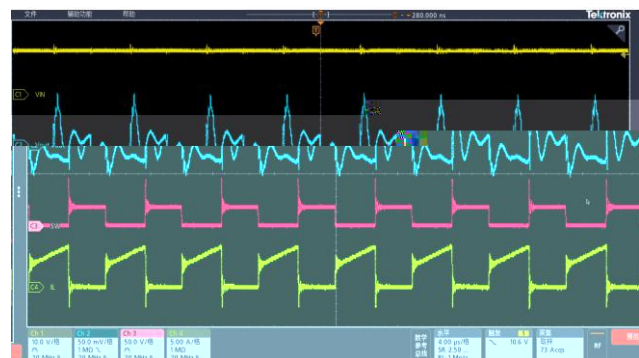
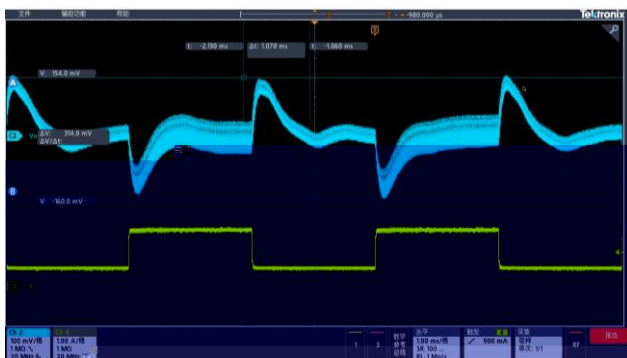
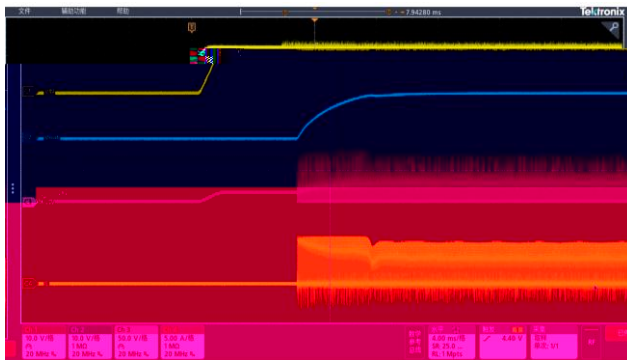
•
•

Input Capacitor Selection

_____ 1

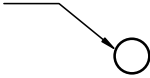
SCT81623Q

Application Waveforms



Layout Guideline

PIN 1 ID
MARKING



PIN 1 ID
INDEX AREA



TOP VIEW

PIN 1 ID
0.25X45°TYP.



BOTTOM VIEW

SIDE VIEW

SECTION A-A

NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO-220.
- 6) DRAWING IS NOT TO SCALE.

RECOMMENDED LAND PATTERN

Dimension A