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- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Wide Input Voltage Range:
  - 3.0V-40V with pre-boost regulator
  - 6.0V-40V without pre-boost regulator
- Asynchronous Pre-Boost Controller VO_BST:
  - Fixed Output Voltage of 7.5V
  - Maximum Duty Cycle up to 95%
  - Fixed 500kHz Switching Frequency
- Synchronous Pre-Buck1 Converter VO_BUCK1:
  - Fixed Output Voltage of 5.8V/5V/4V/3.3V
  - Up to 1.8A Continuous Output Current
  - Integrated 280 -Side and 90 Low-Side Power MOSFETs
  - Selectable 400kHz or 2.2MHz Switching Frequency
- LDO1 VO_UC for µC Supply:
  - Selectable 5V/3.3V/1.8V Output Voltage
  - +/- 2% Output Voltage Accuracy
  - Up to 800mA Continuous Output Current
- LDO2 VO_COM for Communication Supply:
  - Selectable 5V/3.3V/1.8V Output Voltage
  - +/- 2% Output Voltage Accuracy
  - Up to 600mA Continuous Output Current
- Dual Tracker LDO3,4 VO_TRK1, VO_TRK2:
  - +/- 1% Accuracy under 5V Output Voltage or +/- 10mV Accuracy under tracking mode
  - Selectable 5V/3.3V/1.8V or VREF tracking mode Output Voltage
  - Up to 150mA Continuous Output Current
- LDO5 VO_VREF for Voltage Reference:
  - Selectable 5V/3.3V/1.8V Output Voltage
  - +/- 1% Output Voltage Accuracy
  - Up to 200mA Continuous Output Current
- LDO6 VO_STB for Standby Supply:
  - Selectable 3.3V or 5V Output Voltage
  - +/- 4% Output Voltage Accuracy
  - Up to 20mA Continuous Output Current
- Integrated Frequency Dither for EMI Mitigation
- Safe State Outputs SS1, SS2
- Reset Output RESETB for System Management
- Interrupt Output INTB
- Independent External Voltage Monitor
- Error Signal Input Monitoring

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 0.6: Customer Preview

Revision 0.8: Customer Sample

Revision 0.81: Correct typo

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PART NUMBER	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DISCRIPTION	MSL
SCT61480S-xxxxQFFR(1)	Tape & Reel	3000	1480S	48	QFN7x7-48L	3

1) For Tape & Reel, Add Suffix R (e.g. SCT61480S-xxxxQFFR)
"xxxx" is the specific suffix code for different configuration, contact SCT for details

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Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	42	V
SW_BK1	-0.3(-1V trans 30ns)	42	V
VO_BK1, VIN_LDO	-0.3	7	V
Others	-0.3	6	V
Junction temperature(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 175°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

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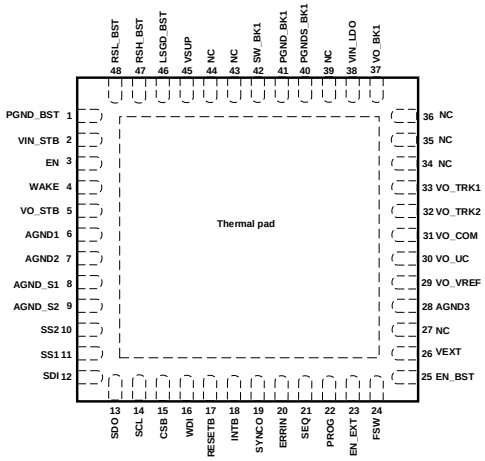

Top View: 48-Lead QFN 7mmx7mmC

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NAME	NO.	DESCRIPTION
PGND_BST	1	Boost driver ground. Connect this pin to ground at the low side of Boost external current sense resistor to decouple the driver noise from the sensitive ground. If Boost is not used, connect this pin to ground directly.
VIN_STB	2	Standby LDO voltage input. Connect this input to supply (battery) voltage with reverse protection diode and capacitor between pin and ground. An EMC filter is recommended.
EN	3	Enable Input. A positive edge signal at this pin will wake the device. Connect to ground if not used.
WAKE	4	Wake Input. A high level signal of defined length at this pin will wake the device. In case of not used, connect to ground.
VO_STB	5	Output standby LDO. Connect a capacitor as close as possible to pin.
AGND1	6	Analogue ground, pin 1. Connect this pin directly (low ohmic and low inductive) to ground.
AGND2	7	Analogue ground, pin 2. Connect this pin directly (low ohmic and low inductive) to ground.
AGND_S1	8	Analogue ground, safety, pin 1. Connect this pin directly (low ohmic and low inductive) to ground. In case a safety switch is used, connect directly to the source of the NMOS used.
AGND_S2	9	Analogue ground, safety, pin 2. Connect this pin directly (low ohmic and low inductive) to ground. In case a safety switch is used, connect directly to the source of the NMOS used.
SS2	10	Safe state output signal 2, sets the application into a safe state. Signal is delayed against SS1, delay can be adjusted via SPI command.
SS1	11	Safe state output signal 1, sets the application into a safe state.
SDI	12	Serial peripheral interface, signal data input. SPI signalling port, connect to SPI port “data output” of micro processor to receive commands during SPI communication.
SDO	13	Serial peripheral interface, signal data output. SPI signalling port, connect to SPI port “data input” of micro processor to send status information during SPI communication. If not used, leave open.
SCL	14	Serial peripheral signal clock. SPI signalling port, connect to SPI port “clock” of micro processor to clock the device for SPI communication.
CSB	15	Serial peripheral interface, signal chip select. SPI signalling port, connect to SPI port “chip select” of micro processor to address the device for SPI communication. If not used, leave open.
WDI	16	Watchdog input, trigger signal. Input for trigger signal, connect the “trigger signal output” of the micro processor to this pin. In case of not used, leave open (internal pull-down).
RESETB	17	Reset output. Open drain structure with internal pull-up current source. A low signal at this pin indicates a reset event.
INTB	18	Interrupt signal. Push-pull-stage. A low pulse at this pin indicates an interrupt, the micro processor shall read out the SPI status registers. Connect to a non maskable interrupt port (NMI) of the micro processor core supply voltage.
SYNCO	19	Synchronization output signal. Connect this output to the optional external switch mode post regulator synchronization input. The signal delivers the buck regulator switching frequency either in phase or shifted by 180° (selectable via SPI command). The switch mode post regulator shall synchronize to the rising edge. If not used, leave open.

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NAME	NO.	DESCRIPTION
PGND_BK1	41	Pre-Buck1 power ground. Connect this pin straight (low ohmic and low inductive) to ground and pre regulator output capacitor minus. Always connect in parallel with pin PGND1S.
SW_BK1	42	Pre-Buck1 switching node. Connect this pin straight (low ohmic and low inductive) to the pre regulator output filter.
NC	43	Internally not connected: This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
NC	44	Internally not connected. This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
VSUP	45	Power supply voltage Pre-Buck1 regulator input. Connect this input to the output of the boost pre regulator. If boost pre regulator option is not used, connect to supply (battery) voltage with reverse protection diode and capacitor between pin C and ground. An Ee s

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Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{BAT}	Operating Voltage Range with active Pre-Boost	3.0	40	V
T_J	Operating Junction Temperature	-40	150	°C

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PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC-Q100-002	-2	2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	1	kV

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PARAMETER	THERMAL METRIC	QFN-48	UNIT
R	Junction to ambient thermal resistance(1)	25.06	°C/W
JT	Junction-to-top characterization parameter	3.49	
JB	Junction-to-board characterization parameter(1)	9.1	
R (top)	Junction to case (top) thermal resistance(1)	19.5	
R B	Junction to board thermal resistance(1)	9.53	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT61480S is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT61480S. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

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V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{SUP}	Operating input voltage at VSUP pin		6		40	V
V_{SUP_UVLO}	Input UVLO	V_{SUP} rising	4.35	4.6	4.85	V
$V_{SUP\_UVLO\_HYS}$	Hysteresis			1.6		V
V_{SUP_OVP}	Input OVP	V_{SUP} rising	42	44	46	V
$V_{SUP\_OVP\_HYS}$	Hysteresis		1	2	3	V
$V_{START,STG,BUCK\_RISING}$	Step down regulator short to ground activation rising threshold at pin VSUP	V_{SUP} increasing	5.5	5.7	5.9	V
$V_{START,STG,BUCK\_HYS}$	Step down regulator short to ground activation threshold Hysteresis at pin VSUP			150		mV

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V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
R_{DIS_VUC}	Discharge resistance	Output disabled, 1.8V<V_{O_UC}<6V		50		
LDO2 VCOM						
V_{O_COM}	VCOM output voltage	0mA ≤ I_{VCOM} ≤ 300mA	4.9	5	5.1	V
			3.23	3.3	3.37	V
I_{LIM_VCOM}	Output current limit		650	850	1100	mA
V_{DROP_VCOM}	Dropout voltage	0 mA ≤ I_{VCO} ≤ 300 mA			220	mV
		0 mA ≤ I_{VCO} ≤ 600 mA			550	mV
ΔV_{VCOM}	Load regulation	I_{VUC} to 300mA			10	mV
		I_{VUC} to 600mA			10	mV
$PSRR_{VCOM}$	Power supply ripple rejection	V_{O_BK1} = 5.8V, $ESRC_{VCOM}$≤ C_{VCOM}=10 $_{VCOM}$ 100mA, f = 1kHz to 1MHz	26			dB
C_{VCOM}	Output capacitor		1		47	
$ESRC_{VCOM}$	Output capacitor, ESR		1		200	
T_{OT_WRN}	Over Temperature Warning Threshold		130	140	150	
T_{OT_SD}	Over Temperature Shutdown Threshold		160	180	200	
T_{OT_HYS}	Over Temperature Sensor Hysteresis		-	10	-	
t_{SS_VCOM}	Soft-start time	C_{O_COM} $_{O\_COM}$ rising from 10% to 90%	130	200	270	
R_{DIS_VCOM}	Discharge resistance	Output disabled, 1.8V<V_{O_COM}<6V		60		
LDO5 VREF						
V_{O_VREF}	VREF output voltage	0mA ≤ I_{VREF} ≤ 200mA	4.95	5	5.05	V
I_{LIM_VREF}	Output current limit		250	300	350	mA
V_{DROP_VREF}	Dropout voltage	0 mA ≤ I_{VREF} ≤ 150mA			400	mV
		0 mA ≤ I_{VREF} ≤ 200mA			450	mV
ΔV_{VREF}	Load regulation	I_{VREF}		4.5	9	mV
$PSRR_{VREF}$	Power supply ripple rejection	V_{O_BK1} = 5.8V, $ESRC_{VREF}$≤ C_{VREF}=10 $_{VREF}$ 100mA, f = 1kHz to 1MHz	26			dB
C_{VREF}	Output capacitor		1		10	
$ESRC_{VREF}$	Output capacitor, ESR		0		200	
t_{SS_VREF}	Soft-start time	C_{O_VREF} $_{O\_VREF}$ rising from 10% to 90%	130	200	270	

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V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
R_{DIS_VREF}	Discharge resistance	Output disabled, 1.8V<V_{O_VREF}<6V		60		
Tracker LDO3,4 VTRK1, VTRK2						
ΔV_{O_TRKx}	Output voltage tracking accuracy to voltage reference Output Accuracy in 5V Mode	0mA ≤ I_{VTRKx} ≤ 200mA	-10		10	mV
		0mA ≤ I_{VTRKx} ≤ 200mA	-1		1	%
I_{LIM_VTRKx}	Output current limit		250	350	450	mA
V_{DROP_VTRKx}	Dropout voltage	0 mA ≤ I_{VTRKx} ≤ 200 mA			400	mV
ΔV_{VTRKx}	Load regulation	I_{VQTx}		4.5	9	mV
$PSRR_{VTRKx}$	Power supply ripple rejection	V_{O_BK1} = 5.8V, $ESRC_{VTRKx}$≤ C_{VTRKx}=10 $_{VTRKx}$ 100mA, f = 1kHz to 1MHz	26			dB
C_{VTRKx}	Output capacitor		1		10	
t_{SS_VTRKx}	Soft-start time	C_{O_TRKx} $_{O\_TRKx}$ rising from 10% to 90%	130	200	270	
R_{DIS_VTRKx}	Discharge resistance	Output disabled, 1.8V<V_{O_TRKx}<6V		10		k
Standby LDO6 VSTB						
V_{O_STB}	VSTB output voltage	V_{VSTB} = 5V,0mA ≤ I_{VSTB} ≤ 20mA	4.9	5	5.1	V
		V_{VSTB} = 3.3V,0mA ≤ I_{VSTB} ≤ 20mA	3.2	3.3	3.4	V
I_{LIM_VSTB}	Output current limit		45	60	75	mA
V_{DROP_VSTB}	Dropout voltage	V_{VSTB} = 5V, I_{VSTB} to 20mA			500	mV
ΔV_{VSTB_LOAD}	Load regulation	V_{VSTB} = 5V, I_{VSTB} to 20mA			20	mV
		V_{VSTB} = 3.3V, I_{VSTB}			20	mV
ΔV_{VSTB_LINE}	Line regulation	V_{VSTB} = 5V		0.1	0.5	mV/V
		V_{VSTB} = 3.3V		0.1	0.5	mV/V
$PSRR_{VSTB}$	Power supply ripple rejection	$ESRC_{VSTB}$≤ $_{VSTB}$ =10 $_{VSTB}$ 100mA, f = 100kHz	40			dB
C_{VSTB}	Output capacitor		0.47		10	
$ESRC_{VSTB}$	Output capacitor, ESR		0		200	
t_{SS_VSTB}	Soft-start time	C_{O_VSTB} 2.2 $_{O\_VSTB}$ rising from 10% to 90%	130	200	270	
R_{DIS_VSTB}	Discharge resistance	Output disabled, 1.8V<V_{O_VSTB}<6V		50		
External Regulator						
V_{SEQ_H}	SEQ high level	V_{VUC} = 5.0 V, I_{EN_EXT} = -9 mA	4			V

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V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT

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V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
RESETB OV/UV Threshold for LDO VREF						
$V_{OV\_THR\_VREF}$	Over voltage reset threshold	5V output, option 0	105	107	109	%
		5V output, option 1	102	104	106	%
		3.3V output, option 0	105	107	109	%
		3.3V output, option 1	104	106	108	%
$V_{OV\_HYS\_VREF}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
$V_{UV\_THR\_VREF}$	Under voltage reset threshold	5V output, option 0	84	86	88	%
		5V output, option 1	95	96	97	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	92	94	96	%
$V_{UV\_HYS\_VREF}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
RESETB OV/UV Threshold for Tracker VTRK1						
$V_{OV\_THR\_VTRK1}$	Over voltage reset threshold	5V output, option 0	108	110	112	%
		5V output, option 1	106	108	110	%
		3.3V output	105	107	109	%
$V_{OV\_HYS\_VTRK1}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
$V_{UV\_THR\_VTRK1}$	Under voltage reset threshold	5V output, option 0	88	90	92	%
		5V output, option 1	90	92	94	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	90	92	94	%
$V_{UV\_HYS\_VTRK1}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
RESETB OV/UV Threshold for Tracker VTRK2						
$V_{OV\_THR\_VTRK2}$	Over voltage reset threshold	5V output, option 0	108	110	112	%
		5V output, option 1	106	108	110	%
		3.3V output	105	107	109	%
$V_{OV\_HYS\_VTRK2}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV

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V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{UV_THR_VTRK2}$	Under voltage reset threshold	5V output, option 0	88	90	92	%
		5V output, option 1	90	92	94	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	90	92	94	%
$V_{UV_HYS_VTRK2}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
RESETB OV/UV Threshold for Pre-Buck1						
$V_{OV_THR_VBK1}$ VOV_THR_OB113	Over voltage reset threshold		111	113	115	VOV_02.518ol

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V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{INTB_RISE}(2)	INTB output rise time	C_{INTB} = 50pF			25	ns
t_{INTB_FALL}(2)	INTB output fall time	C_{INTB} = 50pF			25	ns
State Machine						
t_{INIT}	INIT timer / Initialization time-out		550	600	650	ms
$t_{FAILSAFE}$	FAILSAFE time		18	20	22	ms
$t_{FAILSAFE\_TSD}$	FAILSAFE time TSD	Thermal shutdown	0.9	1	1.1	s
t_{TR_DEL}	Transition delay timer accuracy		-20		20	%
I_{VUC_ATT}	VUC current monitoring for low power states	10mA monitor current	-60		60	%
		30mA monitor current	-40		40	%
		60mA monitor current	-35		35	%
		100mA monitor current	-30		30	%
t_{TRANS}	State transition time	Except transitions to SLEEP, to STANDBY or from STANDBY			100	
t_{TRANS_INIT}	State transition time to INIT	Except transitions from STANDBY, FAILSAFE and POWERDOWN			150	
		From STANDBY, FAILSAFE and interrupted transition to STANDBY			250	
t_{ST_PWD}	Internal start-up time from POWERDOWN	From first VS connection to INIT/ power sequence		0.4	2	ms
ERRIN Pin						
V_{ERR_H}	ERRIN valid high level	V_{VUC} = 5V	3.6			V
		V_{VUC} = 3.3V	2			V
V_{ERR_L}	ERRIN valid low level				0.8	V
V_{ERR_HYS}	ERRIN hysteresis	V_{VUC} = 5V		350		mV
		V_{VUC} = 3.3V		160		mV
I_{ERR_PULL}	ERRIN pull-down current			150	330	A

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V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{WD_SAMPLE}	Watchdog sampling time		188	200	213	s
V_{WDI_HI}	Threshold for WDI pin	WDI voltage rising, V_{VUC} = 5V	3.6			V
		WDI voltage rising, V_{VUC} = 3.3V	2			V
V_{WDI_LOW}	Threshold for WDI pin				0.8	V
V_{WDI_HYS}	WDI Hysterisis	V_{VUC} = 5V		350		mV
		V_{VUC} = 3.3V		160		mV
I_{WDI_PULL}	WDI pull-down current			150	330	A
R_{WDI}(2)	WDI input capacitance			4	15	pF
$t_{WDI\_DEG\_RISING}$	Deglitch time for WDI pin	WDI voltage rising		30		s
t_{WD}	Watchdog timer accuracy		-8		8	%
Wake up Timer						
t_{WAKE_TR}	Wake up timer	Option0	9.5	10	10.5	s
		Option1	9.5	10	10.5	ms
		Option2	0.95	1	1.05	s
C_{WAKE}	Counter			24		bit
SPI Interface (CSB, SCL, SDO, SDI)						
$V_{CSB,High}$	CSB Pin High Voltage Level	V_{VUC}=5V	3.6			V
		V_{VUC}=3.3V	2			V
$V_{CSB,Low}$	CSB Pin Low Voltage Level				0.8	V
$V_{CSB,\ Hys}$	CSB Pin Hysteresis	V_{VUC}=5V		350		mV

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V_{IN} = 12V, V_{Buck1} = 5.8V, V_{LDO1} ~ V_{LDO6}= 5V, L1 = 10uH, T_A = 25°C, unless otherwise noted.

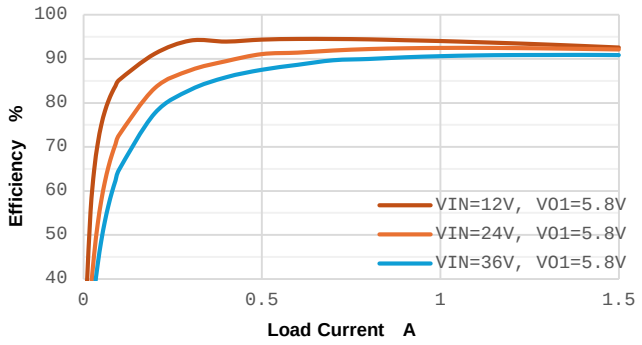

Figure 1. Buck1 Efficiency vs. Load Current(400kHz)

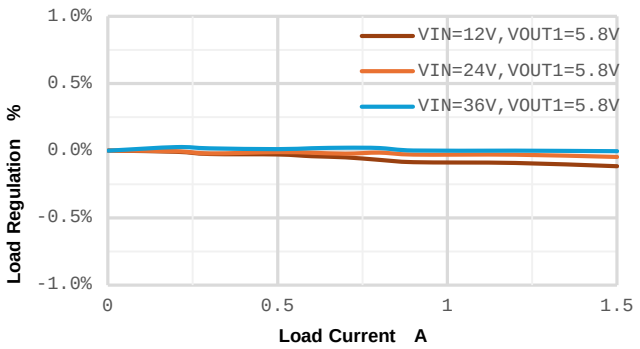

Figure 2. Buck1 Load Regulation

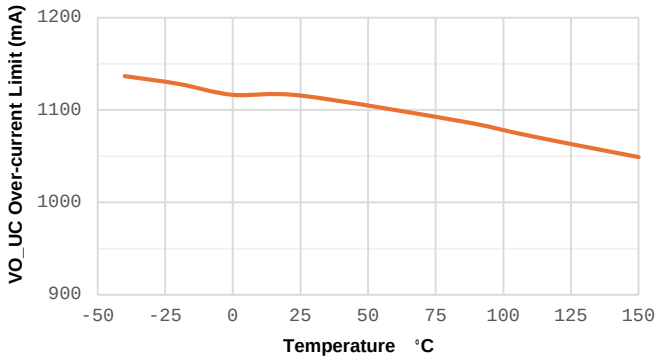

Figure 3. VO-UC Over-current Limit vs. Temperature

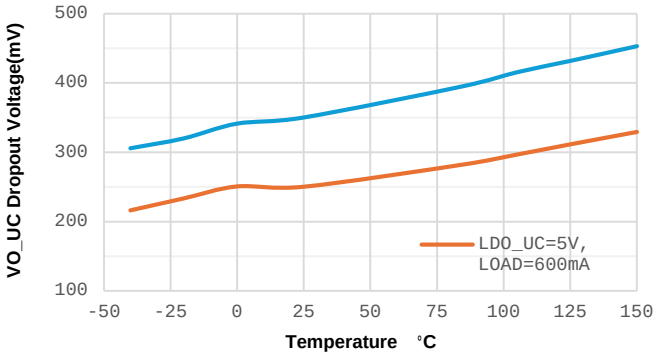

Figure 4. VO-UC Dropout Voltage vs. Temperature

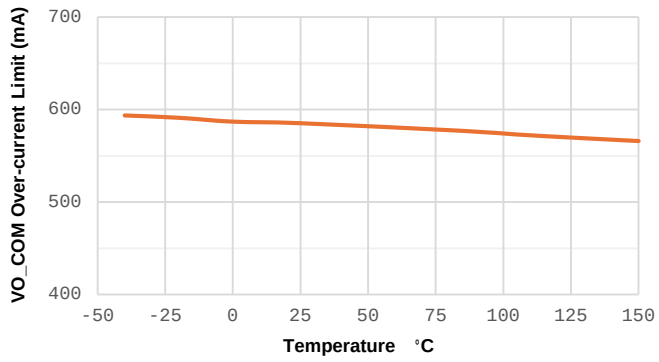

Figure 5. VO-COM Over-current Limit vs. Temperature

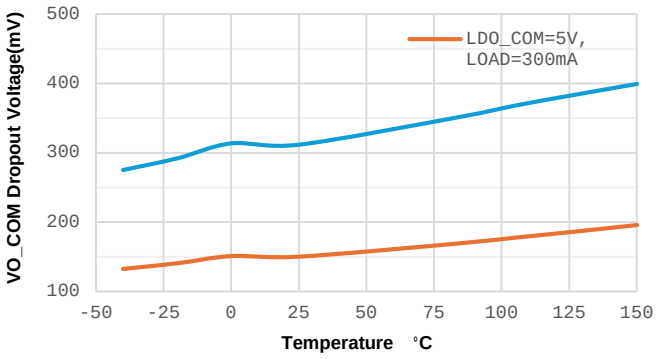

Figure 6. VO-COM Dropout Voltage vs. Temperature

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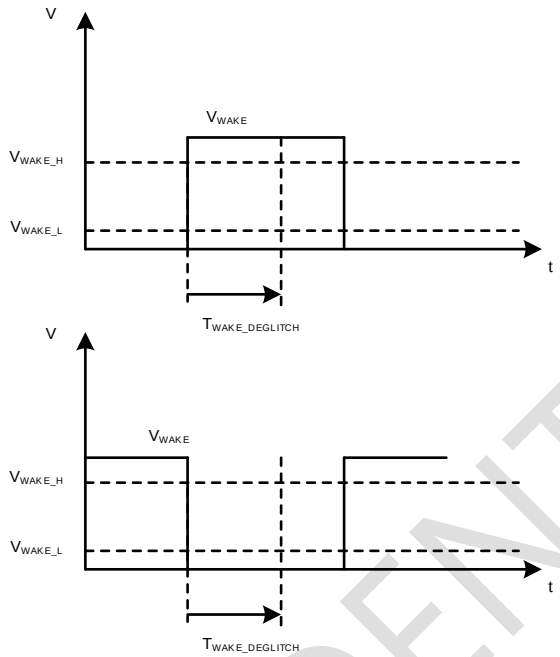

Figure 15. Valid wake signal

A valid

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SPI.
For the chosen time-base is 1 s and a wake up time between 1 s to 194 days can be configured via SPI.
When entering STANDBY or SLEEP state, the counter is loaded with the value of the wake up timer register and starts decrementing. At underflow, the timer will wake up the device from either SLEEP or STANDBY state. When leaving SLEEP state, an interrupt will be generated. The remaining timer counter will be stored if the device wake up before the timer is expired, MCU can read back via SPI to calculate the corresponding time elapsed.

3 Pre Regulators

3.1 Introduction

The pre regulator is mandatory to maintain a stabilized and constant intermediate circuit voltage to supply the following post regulators. It consists of two independent regulators: A HV boost converter with an external power stage in front to maintain a minimum input voltage to the following HV buck converter.
The boost converter can be deactivated (if not needed) by connecting pin EN_BOOST to ground. Leaving pin EN_BOOST open activates the boost regulator.
The buck regulator frequency can be preset by leaving pin FSW open for the high switching frequency range or connecting to GND for the low switching frequency range.
The HV buck converter is constantly on, providing a stabilized intermediate circuit voltage VO_BK1 to supply the following post regulators. The boost converter is connected directly to the input voltage V_{Bat}. It only operates during low input voltage condition (i.e. cold crank) when the input voltage drops below the threshold $V_{PRE\_REG,boost,UV}$, to maintain an input voltage high enough for the foll13.1 (he)0-6..181 -1.22

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3.2 HV Boost Regulator

The asynchronous boost pre regulator provides a higher output voltage than the input voltage when operating. This will be the case whenever the supply voltage should be too low to allow nominal values at the post regulator outputs. The boost pre regulator output voltage will be well below the nominal supply (battery) voltage to make sure, that he only operates during low input voltage conditions.
If the boost feature should not be necessary for the application, the external power elements (Mosfet, diode) could be skipped, the filter elements might be adjusted to the application requirements.

3.3 HV Buck Regulator

The synchronous buck pre regulator is continuously in operation providing a stable intermediate circuit voltage to supply the following post regulators. The internal power stage consists of synchronous N-channel (high side) and N-channel (low side) Mosfets. For startup a soft start function is implemented.
The regulation loop operates in peak current mode.
Under normal load conditions the regulator operates in Forced continuous conduction mode (FCCM). Under light load conditions it will operate in Pulse Frequency Modulation (PFM) to minimize the internal current consumption (only in SLEEP state, not in NORMAL, WAKE or INIT state).
The output filter of the buck regulator has to be sized to ensure a maximum output voltage ripple of 100 mV in order to be in line with the PSRR specified for the post regulators.

3.4 Frequency Setting

The frequency source supplies the boost pre regulator and the buck pre regulator with a constant frequency. The synchronous power switches of the buck pre regulator will switch directly with the frequency f_{OSC}.
The frequency range of the buck pre regulator can be set to the high switching frequency range by leaving pin FSW open or to the low switching frequency range by connected the pin FSW to GND. The switching frequency will be set to the default value of the chosen frequency range. Optionally it can be fine tuned by SPI command (**BCK_FREQ_CHANGE**) or the spread-spectrum option can be activated (**BCK_FRE_SPREAD**).
The switching frequency range of the boost pre regulator is fixed at 500kHz and will be not impacted by FSW pin.
The switching frequency of the buck pre regulator is offered at pin SYNCO for the optional external switch mode
EN_EXT pin is left open.
The synchronization function is not available in PFM mode.
The SCT61480S cannot be synchronized to an external frequency source.

4 Post Regulators

4.1 Introduction

The SCT61480S includes a number of linear low drop post regulators and offers the possibility to connect an

The bandgap 1 for regulator block provides
communications supply LDO and the reference voltage source VO_VREF. The trackers get their reference value from the VO_VREF. The output voltage of trackers 1 and 2 is following the reference voltage source VO_VREF with a small drop.
An additional external post regulator can be added to deliver the core supply for the micro processor. If this option is used the configuration pin EN_EXT must be left open. If the option is not used, pin EN_EXT must be connected to ground. The post regulator is to be connected external and uses its own reference voltage, the input is fed from the pre regulator output voltage VO_BK1. The post regulator is enabled by a high signal at pin SEQ and switched off with a low signal at pin SEQ. A synchronization signal (in phase or shifted by 180 degree with the buck pre regulator signal) is offered at pin SYNCO for usage of a switch mode post regulator. All output voltages of the post regulators are connected to the voltage monitoring function (please refer to chapter **Voltage Monitor**).
In case of an over voltage the related post regulator will be switched off, the shutdown signal is generated by the voltage monitoring function.

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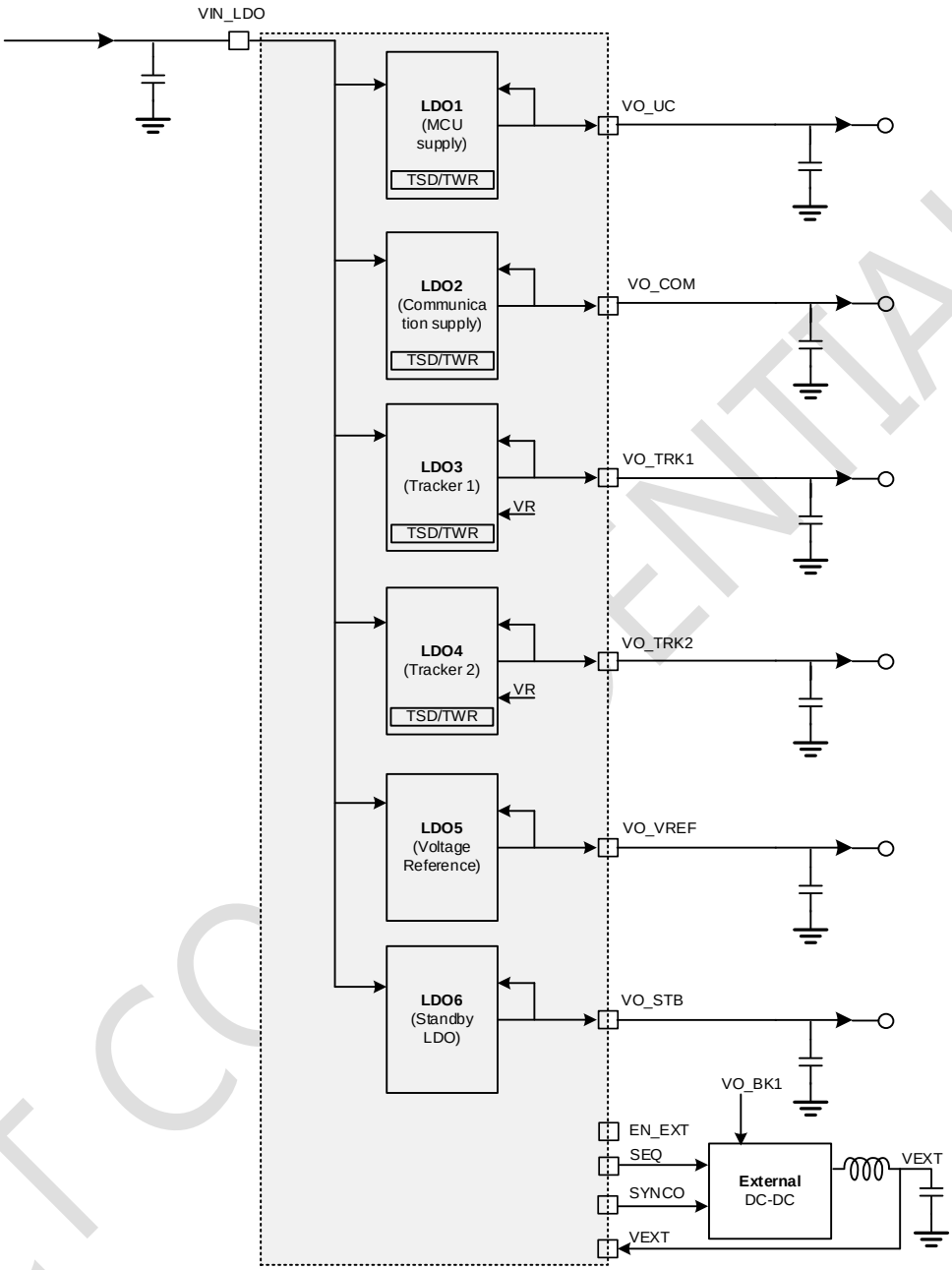

Figure 18. Principle of post regulators

4.2 µ-Processor Supply

offers a precise 3.3 V or 5.0 V output voltage for micro processor supply. The regulator is supplied from the intermediate circuit voltage VO_BK1 which provides a stabilized voltage. The output voltage VO_UC is controlled by the error amplifier. The actual value is compared to a reference voltage derived from band gap 1 for regulators. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR). The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.

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voltage VO_VREF is controlled by the error amplifier. The actual value is compared to a reference voltage derived from band gap 1 for regulators. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR). The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.
Protection circuitry is installed to prevent the regulator and the application from damage:

To protect the pass element of the LDO_VREF from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached the current will be limited, thus the output voltage will decrease. The regulator is protected against short circuit to ground.

The output voltage is monitored by the voltage monitoring. In case of over voltage at pin VO_VREF, the LDO_VREF will be switched off and the device will move into FAILSAFE state. The event will be stored in an SPI status register (**MONSF1**). In case of under voltage at pin VO_VREF, the event will be indicated by an interrupt and stored in an SPI status register (**MONSF2**). The regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{STG}. If the under voltage should be present for more than t_{STG}, the regulator will be switched off. This event will be stored in an SPI status register (**MONSF0**) and an interrupt will be generated.

There is no dedicated temperature sensor for this regulator. The temperature is sensed on the chip by other exceed
the pre warning threshold, an interrupt will indicate this event and it will be stored in a SPI status register (**OTWRNSF**). If the chip temperature will exceed the temperature shutdown threshold, the regulator will be switched off. The temperature switch off time will be at least one second. An overload at LDO LDO_VREF (over current detected for more than 1ms) will be indicated by an interrupt and it will be stored in a SPI status register (**OTWRNSF**).
If the device enters FAILSAFE state the RESETB is pulled low and all supplies are switched off.
The regulator LDO_VREF is switched off in STANDBY and FAILSAFE state. In INIT, SLEEP, NORMAL and WAKE state LDO_VREF is ON or OFF depending on the SPI configuration.
For further details please refer to **Chapter State Machine**.

4.5

The linear trackers 1 and 2 offer a sensor supply with a very high accuracy referred to voltage reference output (pin VO_VREF).
Both trackers are supplied by the intermediate circuit voltage VO_BK1, which provides a stabilized voltage. The output voltage VO_TRKx is controlled by the error amplifier. The actual value is compared to a reference voltage provided by the reference voltage VO_VREF. The tracker output voltages follow the VO_VREF output with a very small drop. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor for each tracker should be chosen according the specified requirements (capacitance value and electrical series resistance ESR). The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.
Protection circuitry is installed to prevent damage to both trackers and the application:

To protect the pass element of a tracker from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached, the current will be limited and in consequence the output voltage will decrease. A tracker is protected against short circuit to ground and short circuit to battery voltage.

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tracker will be switched off, the event will be stored in the SPI status register (**MONSF1**).

There is no dedicated temperature sensor for this regulator. The temperature is sensed on the chip by other

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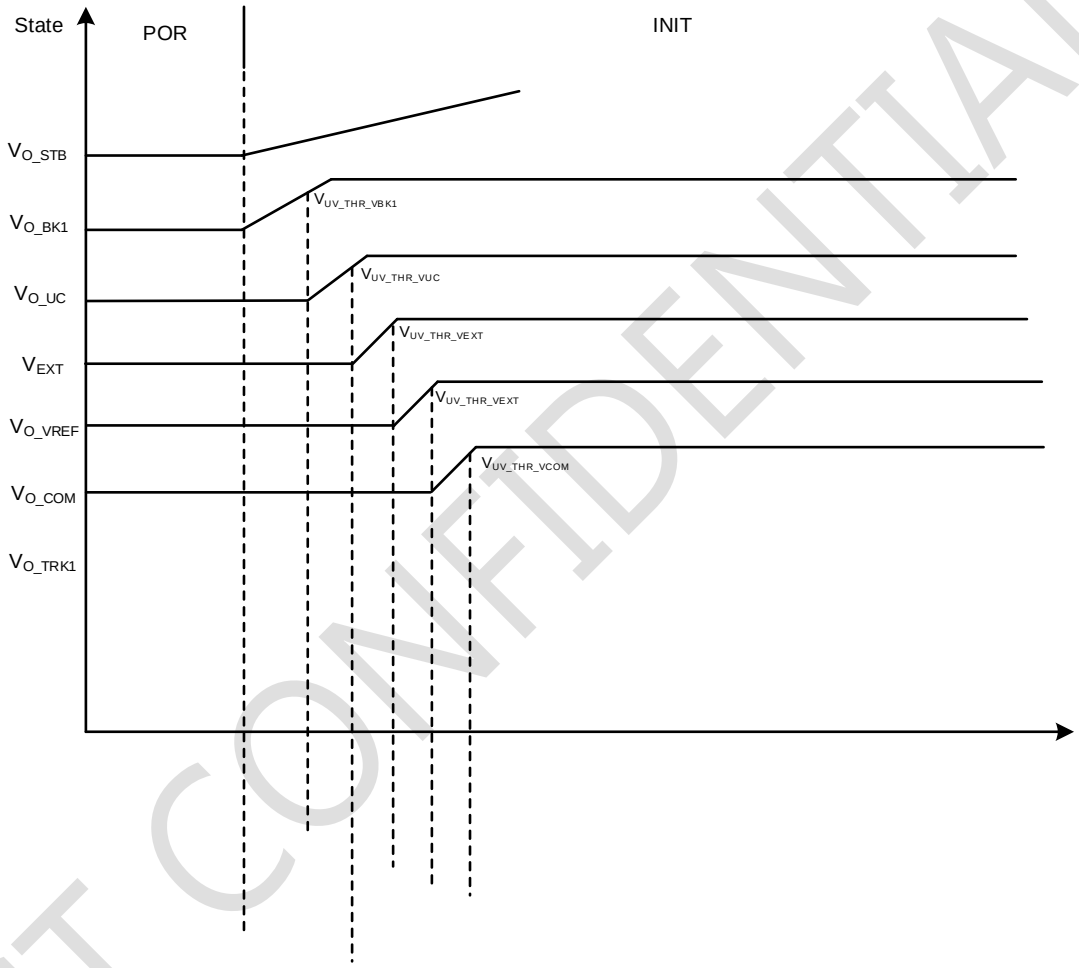
power on reset delay time t_{RD}. The microcontroller should check the status of the outputs by reading the SPI status register (VMONSTAT).
In case the microcontroller is sending a SPI request to enable or disable any non microcontroller related LDO (VO_VREF, VO_COM, VO_TRK1 or VO_TRK2) during the power sequencing, the sequence will be stopped and the requested configuration will be executed.

4.7.1 Power Sequencing from POR to INIT state



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RESETB pin is pulled to high. The figure shows the possibilities of the t_{RD} starting time.
Once the RESETB is high, the microcontroller can change the configuration of the selectable LD1 (g)]TJ(t)-1.1 (53J 04e)0.

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7. When VO_TRK1 is above the lower reset threshold $V_{UV\_THR\_VTRK1}$, the Tracker 2 starts to operate.
8. The reset delay time t_{RD} and the external core supply (if selected) have reached their lower reset threshold. The reset delay time is programmable via SPI. After the rest delay time is expired the RESETB pin is pulled to high. The figure shows the possibilities of the t_{RD} starting time.

4.7.3 Power Sequencing from SLEEP to WAKE state

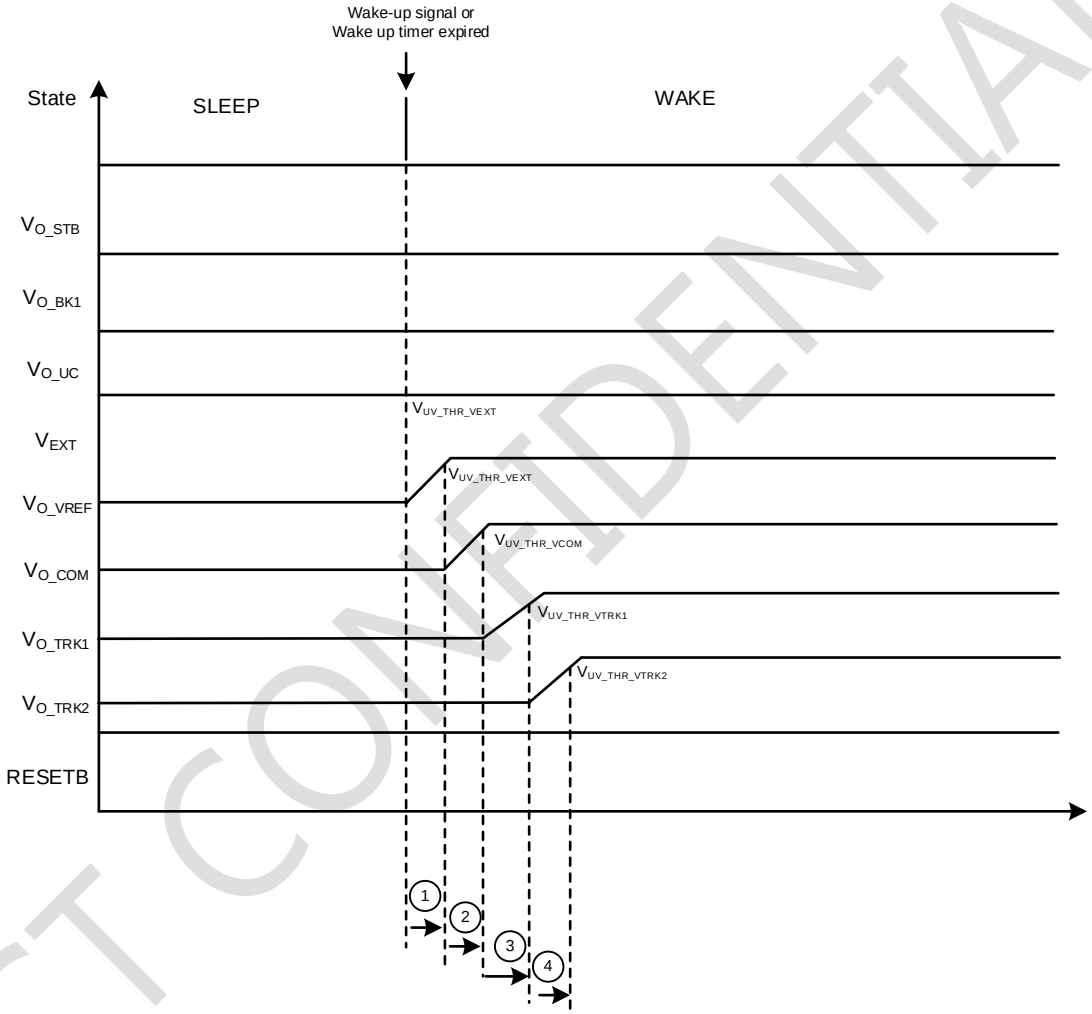

Figure 21. Power sequencing SLEEP to WAKE state

Description: Input voltage is present, device is in SLEEP state, all selectable LDOs switched off in SLEEP state, all selectable LDOs were switched on in previous NORMAL state:
1. After a valid Wake-up signal or an expired wake-up timer the voltage reference starts to operate.
2. When VO_VREF is above the lower reset threshold $V_{UV\_THR\_VREF}$, the LDO_COM starts to operate.
3. When VO_COM is above the lower reset threshold $V_{UV\_THR\_VCOM}$, the Tracker 1 starts to operate.
4. When VO_TRK1 is above the lower reset threshold $V_{UV\_THR\_VTRK1}$, the Tracker 2 starts to operate.
The reset output RESETB is high in SLEEP state and will be kept high for WAKE state.
In case a selectable LDO was switched off in the previous NORMAL state, it will not be enabled during the transition

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VO_COM, VO_TRK1, VO_TRK2), over and under voltage are indicated by an interrupt.

• For the internal supply voltages, over and under voltage are indicated by the hardware reset pin RESETB. In case of an over or under voltage, pin RESETB is pulled to low.

Table 1 Indication Pin Matrix

Regulators	OV Indication Pin	UV Indication Pin	STG Indication Pin
VO_STB	RESETB	RESETB	RESETB
VO_UC	RESETB	RESETB	RESETB
VEXT	RESETB/INTB selectable	RESETB/INTB selectable	RESETB/INTB selectable
VO_BK1	RESETB	INTB	RESETB
VO_COM	INTB	INTB	INTB
VO_VREF	RESETB/INTB selectable	INTB	INTB
VO_TRK1	INTB	INTB	INTB
VO_TRK2	INTB	INTB	INTB
VSUP	RESETB/INTB selectable	RESETB	NA
VCC	RESETB	RESETB	NA
Bandgap1,2	INTB	INTB	NA

5.2 Shutdown Function

A short to ground detection time t_{STG} at the pre regulator output is only active during the power sequence in INIT state. If the output voltage of the pre regulator should not be within the specified limits within a certain time frame, the device will move into FAILSAFE state. There will be no reaction on a detected short to ground once the VO_BK1 is in a valid range after crossing the first time its UV threshold. If the output voltage of the pre regulator should be too low in other cases, the behavior of the device will depend on the voltage monitoring of the post regulators.

The detection of an over voltage at output voltages VO_UC, VEXT, VO_STB, VO_VREF or VO_BK1 will shut down all regulators to protect the loads from harm or destruction and moves the device to FAILSAFE.

The detection of an over voltage at output voltages VO_COM, VO_TRK1, VO_TRK2 will shut down the related regulator to protect the loads from harm or destruction and generate an interrupt event.

If the detected under voltage at output voltages VO_UC, VEXT or VO_STB should be present for more than the short to ground detection time t_{STG}, all regulators will shut down to protect themselves and the chip from over heating and move the device to FAILSAFE.

If the detected under voltage at output voltages VO_VREF, VO_COM, VO_TRK1, VO_TRK2 should be present for more than the short to ground detection time t_{STG}, the related regulator will shut down to protect himself and the chip from over heating and generate an interrupt event.

The detection of an over voltage or under voltage at power supply voltage VSUP, internal supply voltage VCC will shut down all regulators.

Table 2 Shutdown Matrix

Output	OV	UV	STG
VO_STB	All regulators shut down	No shut down	All regulators shut down
VO_UC	All regulators shut down	No shut down	All regulators shut down
VEXT	All regulators shut down/No shutdown, selectable;Assert EN_EXT	No shut down	All regulators shut down/No shutdown, selectable;Assert EN_EXT
VO_BK1	All regulators shut down	No shut down	All regulators shut down
VO_COM	VO_COM shutdown	No shut down	VO_COM shutdown
VO_VREF	All regulators shut down/No shutdown, selectable	No shut down	Related regulators shut down
VO_TRK1	VO_TRK1 shutdown	No shut down	VO_TRK1 shutdown
VO_TRK2	VO_TRK2 shutdown	No shut down	VO_TRK2 shutdown
VSUP	All regulators shut down/No shutdown, selectable	All regulators shut down	NA
VCC	All regulators shut down	All regulators shut down	NA

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5.3 Reset Function

The reset generator starts to operate as soon as the internal POR is released.
It is called a “Soft Reset” if pin RESETB goes low, but the pre and post regulator output voltages are not switched off.
It is called a “Hard Reset” if pin RESETB goes low and the post regulator output voltages are switched off. The power sequencing will be restarted after a delay of t_{SDT}.(Applicable to the second initialization timeout in a row).
The reset output pin RESETB is an open drain structure. As soon as a reset condition occurs, the RESETB pin is pulled low. An internal pull up current is pulling the output towards VO_UC.
The contribution of regulators to reset is shown in Table1. Besides, IBIAS monitoring is contributing to trigger a reset. The IBIAS monitor fault is stored in a status bit (**BIASHI** or **BIASLOW**).

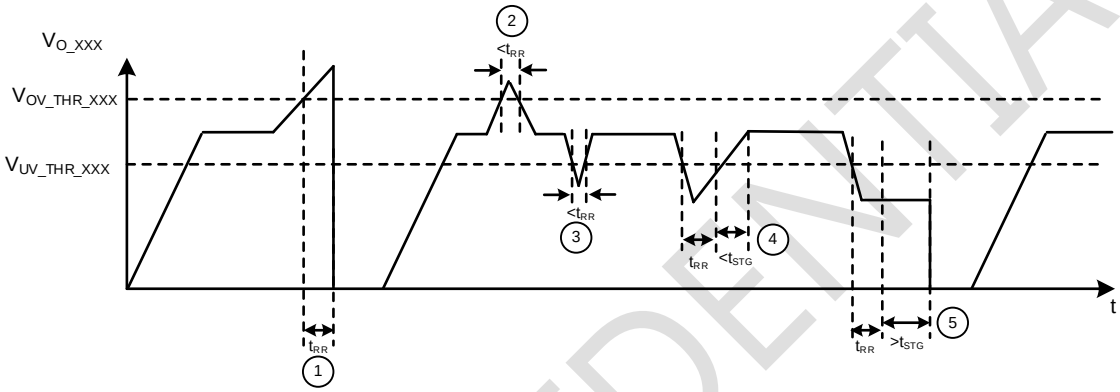

Figure 22. Timing diagram hardware reset signal RESETB for output voltages

1. Voltage exceeds OV threshold and last for longer than t_{RR}, OV event is triggered.

2. Voltage exceeds OV threshold but last for shorter than t_{RR}, OV event is not triggered.

3. Voltage falls below UV threshold but last for shorter than t_{RR}, UV event is not triggered.

4. Voltage falls below UV threshold and last for longer than t_{RR}, UV event is triggered. After UV event is triggered, voltage still lower than UV threshold but last for shorter than t_{STG}, STG event is not triggered.

5.Voltage falls below UV threshold and last for longer than t_{RR}, UV event is triggered. After UV event is triggered, voltage still lower than UV threshold and last for longer than t_{STG}, STG event is triggered.

5.4 Interrupt Function

The interrupt generator starts to operate as soon as the internal POR is released.
Th
VO_COM, VO_TRK1 and VO_TRK2, the pre regulator output voltage VO_BK1 (under voltage only) and the voltage reference output VO_VREF (under voltage and short to ground only). The result is written in a SPI status register (**IF** and **MONSF0**, **MONSF1** or **MONSF2**) and indicated via interrupt (pin INTB). The connection of all these monitoring signals is a logic OR. The interrupt pin INT does not only indicate the result of the voltage monitoring, but also interrupts due to other events in the device.
The interrupt output pin INT is a push pull structure. An interrupt is indicated by pulling the INTB pin to ground. The contribution of regulators to interrupt is shown in Table1.

6 Standby LDO and Internal Supplies

6.1 Standby LDO VO_STB

The standby regulator LDO_STB is independent from the pre regulator stage and the other post regulators. It might

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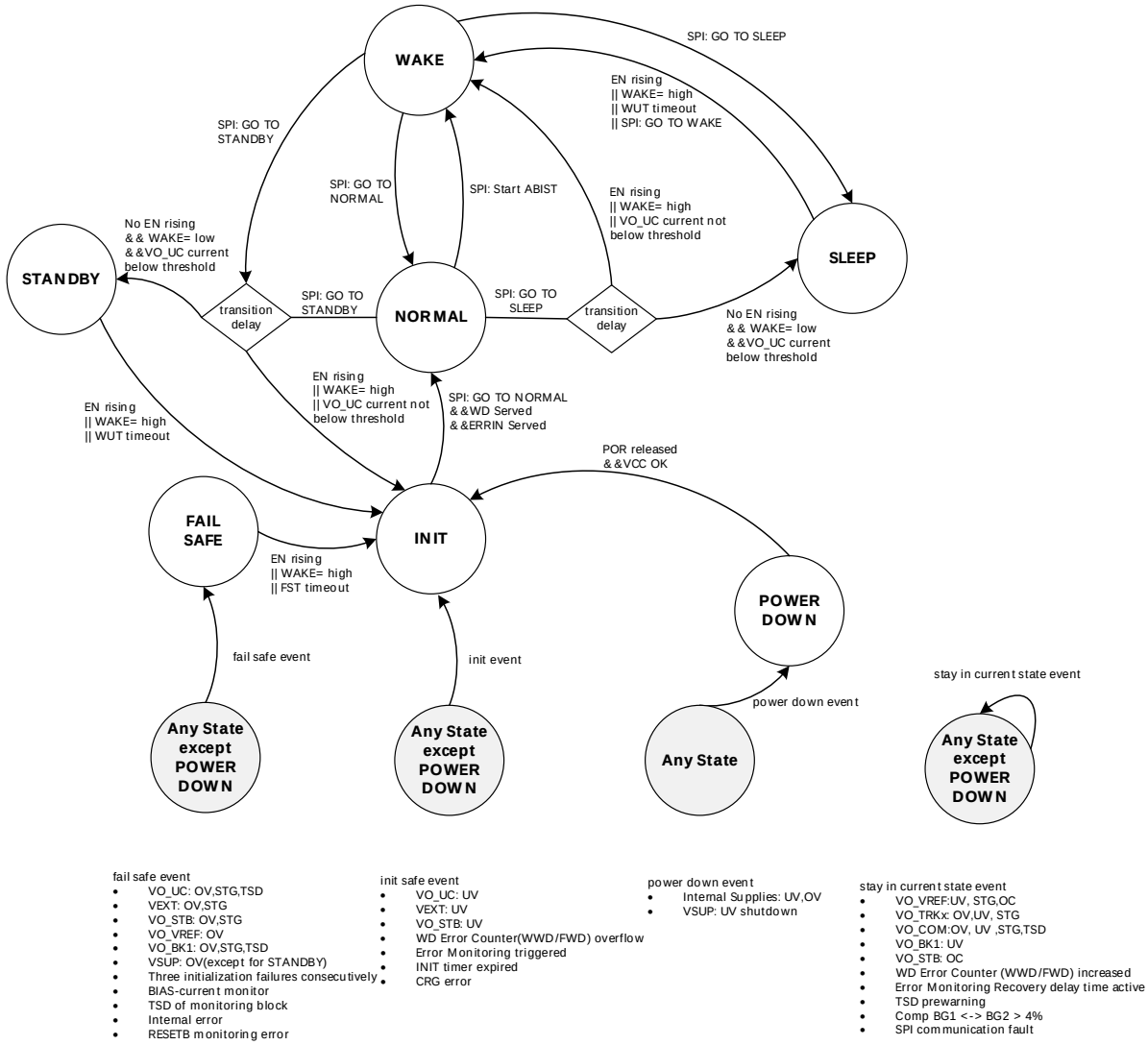

7.2 Detailed Operating States

7.2.1 POWERDOWN state

The device is in POWERDOWN state when supply voltage VSUP is lower than UVLO threshold or internal supplies VCC occurs OV/UV.

Table 3 POWERDOWN Operation State

Block/Function	Status	Description
LDO_STB	OFF	The LDO_STB is off
HV Buck1	OFF	The HV Buck1 is off
	OFF	The is off
External Post Regulator	OFF	The External Post Regulator is off

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7.2.3 NORMAL state

In NORMAL-

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RESETB	LOW	The RESETB pin is low
SS1&SS2	LOW	Both safe state signals are LOW and the application is in safe state

7.2.5 SLEEP state

The device is in POWERDOWN state when supply voltage VSUP is lower than UVLO threshold or internal supplies VCC occurs OV/UV.

Table 7 SLEEP Operation State

Block/Function	Status	Description
LDO_STB	SELECTED	The LDO_STB may be switched on or off depending on its configuration.
HV Buck1	ON	The HV Buck1 is on The boost is active depending on the input voltage and this option is selected by pin EN_BST.
	ON	In SLEEP- current exceeds a certain threshold I_{VUC_ATT} an interrupt will be generated and the device will move to WAKE state
External Post Regulator	ADJUSTED	The External Post Regulator is switched ON or OFF depending on pin EN_EXT (EN_EXT pin considered only during power-sequencing)
LDO_COM	SELECTED	The LDO_COM is switched ON or OFF depending on the configuration by the state transition request to move into SLEEP and cannot be changed in SLEEP state.
LDO_VREF	SELECTED	The LDO_VREF B is switched ON or OFF depending on the configuration by the state transition request to move into SLEEP and cannot be changed in SLEEP state.
LDO_TRK1&2	SELECTED	The LDO_TRK1&2 is switched ON or OFF depending on the configuration by the state transition request to move into SLEEP and cannot be changed in SLEEP state.
Wakeup Timer	SELECTED	The Wakeup Timer may be switched on or off depending on its configuration.
Watchdog	SELECTED	The Watchdog may be switched on or off depending on its configuration.
ERRIN	SELECTED	The Error monitoring may be switched on or off depending on its configuration.
RESETB	HIGH	The RESETB pin is low
SS1&SS2	LOW	Both safe state signals are LOW and the application is in safe state

7.2.6 WAKE state

The WAKE state is an intermediate state between NORMAL and the low power states SLEEP and STANDBY. This state provides the same functionality as the NORMAL state, but shall ensure the application being in safe state by keeping low the safe state outputs. It should be used to prepare the system for a correct and safe reentry to the NORMAL state by servicing the watchdogs and the error monitoring (minimum 3 periods) according to the selected configuration. Furthermore it provides the possibility to move the device into the low power states SLEEP and STANDBY.

The SCT61480S moves from SLEEP or from the transition to SLEEP into WAKE state, if the output current from I_{VUC_ATT}, an valid EN or WAKE signal is recognized or the SPI command GoToWake is sent. Another transition into WAKE state is initiated by the usage of the ABIST in NORMAL state.

By entering the state an interrupt is generated and the supervision functions (watchdogs and ERR monitoring) will become active according to their previous configuration in NORMAL state. Upon entering the WAKE-state the configuration of the LDOs resumes to the one of the previous NORMAL state. The application is in a safe state

Table 8 WAKE Operation State

Block/Function	Status	Description
LDO_STB	SELECTABLE	The LDO_STB may be switched on or off by SPI command.

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RESETB	LOW	The RESETB pin is low
SS1&SS2	LOW	Both safe state signals are LOW and the application is in safe state

7.3 Transition Between States

State transitions requested via SPI command are initiated with a valid positive going edge of the chip select.

7.3.1 POWERDOWN INIT State

The device moves from POWERDOWN to INIT state when the Power-on-Reset (POR) is released. The POR is only released when all of the following conditions are met:

• V_{SUP} above V_{SUP_UVLO} when increasing
• no under or over voltage on internal supplies VCC

7.3.2 INIT NORMAL State

Prerequisites:

• Watchdog(s) need to be serviced once according to default configuration or according to reconfiguration within the INIT timer
• ERR monitor needs to be serviced with a valid signal (minimum 3 periods) or disabled within the INIT timer.
• If functional watchdog is activated, a valid FWD triggering needs to be provided.

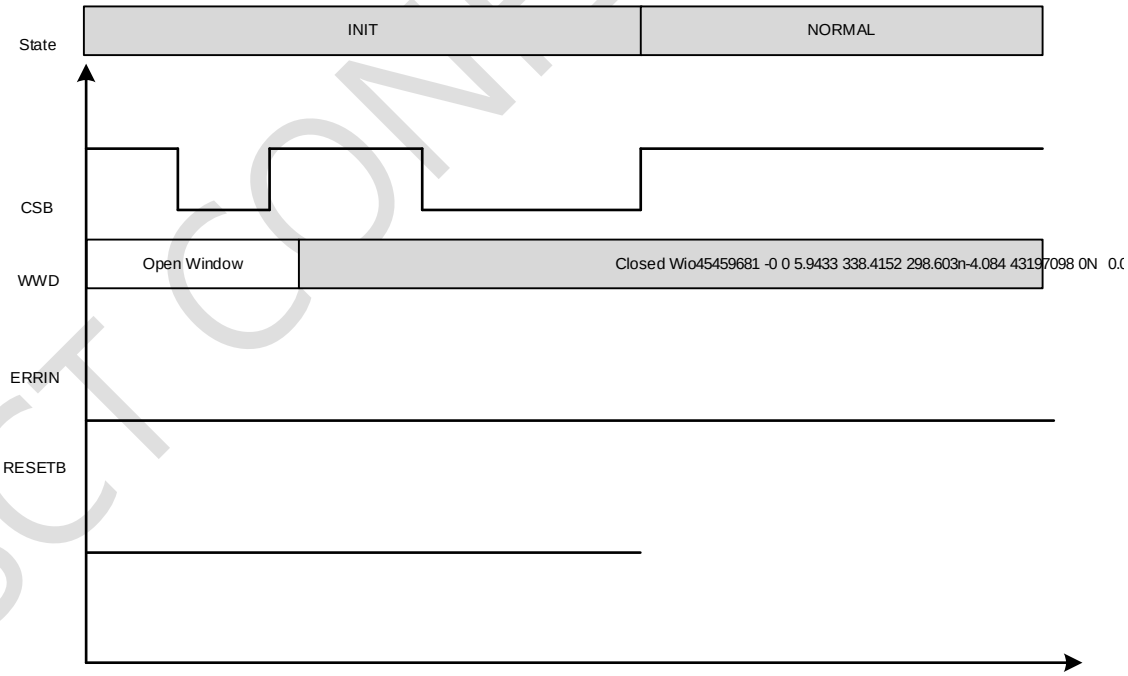
elease of internal validation signals.

Triggering Events:

• State transition is only initiated by the SPI command “Go to NORMAL”.

Exceptions:

• none



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• The state transition is completed without a transition time and is indicated by an interrupt at pin INTB. The triggering event for the transition from SLEEP can be read from the status register **WKSF**.
• All three monitoring functions (window watchdog, functional watchdog and error monitoring) will recover to the condition active or inactive (switched off) as they were in the NORMAL state previous to the SLEEP state.
• The configuration of the LDOs will recover to the condition active or inactive (switched off) as they were in the NORMAL state previous to the SLEEP state.
• In case the window watchdog was active in the previous NORMAL state, with the negative edge of interrupt signal (at pin INTB) the window watchdog will open the first Open Window, the time of this first Open Window depends on the configured cycle time and is 600 ms (**WDCYC** = 1) or 60 ms (**WDCYC** = 0) (if the window watchdog has not been active in SLEEP state) and requires service. If the window watchdog has been active in SLEEP state continuos service is mandatory.
• In case the functional watchdog was active in the previous NORMAL state, with the negative edge of interrupt signal (at pin INTB) the functional watchdog will start the heartbeat timer and require service. If the functional watchdog has been active in SLEEP state continuos service is mandatory.
• In case the ERRIN pin monitoring was active in the previous NORMAL state, with the negative edge of interrupt signal (at pin INTB) the error monitoring will become active again. Latest 10 ms after the activation a toggling signal (with at least three periods past) at pin ERRIN is required. If the error monitoring has been active in SLEEP state continuos toggling is mandatory.
• Reset pin RESETB stays HIGH as the post regulators are active in SLEEP state and in WAKE state.
• The safe signals SS1 and SS2 will stay LOW in SLEEP and in WAKE state.
• If all active monitoring functions (window watchdog, functional watchdog and error monitoring) are serviced properly in WAKE state, you may stay in WAKE state as long as you want.
• If all three monitoring functions (window watchdog, functional watchdog and error monitoring) are inactive (switched off) in WAKE state, you may stay in WAKE state as long as you want.

7.3.5 WAKE SLEEP State

Prerequisites:

• Transition delay timer t_{TR_DEL} needs to be configured or default is used.

Triggering Events:
• State transition is only initiated by the SPI command “Go to SLEEP”.
Exceptions:
• If a valid EN (edge) or WAKE (level) signal is detected in the transition state to SLEEP state, the device will move back to the WAKE state and send an interrupt (at pin INTB)

t_{TR_DEL} has expired, the device will move back to the WAKE state and send an interrupt (at pin INTB)

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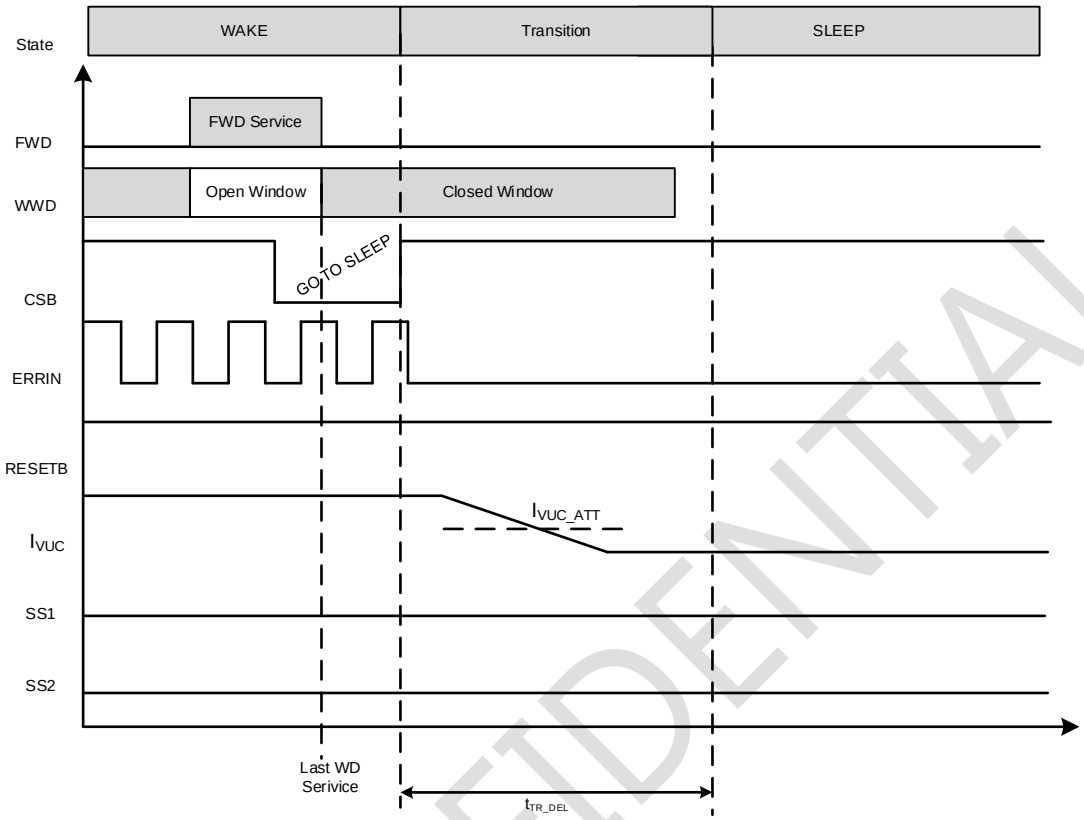

Figure 26. Transition from WAKE to SLEEP state

• Before the SPI command “Go to SLEEP” is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of CSB signal is well in between the “closed window” of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command “Go to SLEEP”
• The positive edge of chip select (pin CSB) after the SPI command “Go to SLEEP” initiates the transition. With chip select high the device leaves WAKE state and enters the transition state (to SLEEP state).
• With chip select (pin CSB) high the error monitoring (pin ERRIN) is stopped - the toggling may end with the positive edge at pin CSB. If the error monitoring should be selected to be active in SLEEP state continuos toggling is mandatory.
• The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin CSB. If one or both watchdogs should be selected to be active in SLEEP state continuos watchdog service is mandatory.
• Reset pin RESETB stays HIGH as the post regulators are not switched off.
VO_UC must fall below th monitoring threshold I_{VUC_ATT} within the configured maximum transition delay time t_{TR_DEL}. The time for the transition is I_{VUC_ATT}, if it is below the transition is done.
• Safe state signals SS1 and SS2 stay LOW all the time.

7.3.6 NORMAL STANDBY State

Prerequisites:

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Exceptions:

• If a valid EN (edge) or WAKE (level) signal is detected in the transition state to STANDBY state, the device will move to the INIT state and a reset is generated.

current threshold before the transition delay timer t_{TR_DEL} has expired, the device will move to the INIT state and a reset is generated

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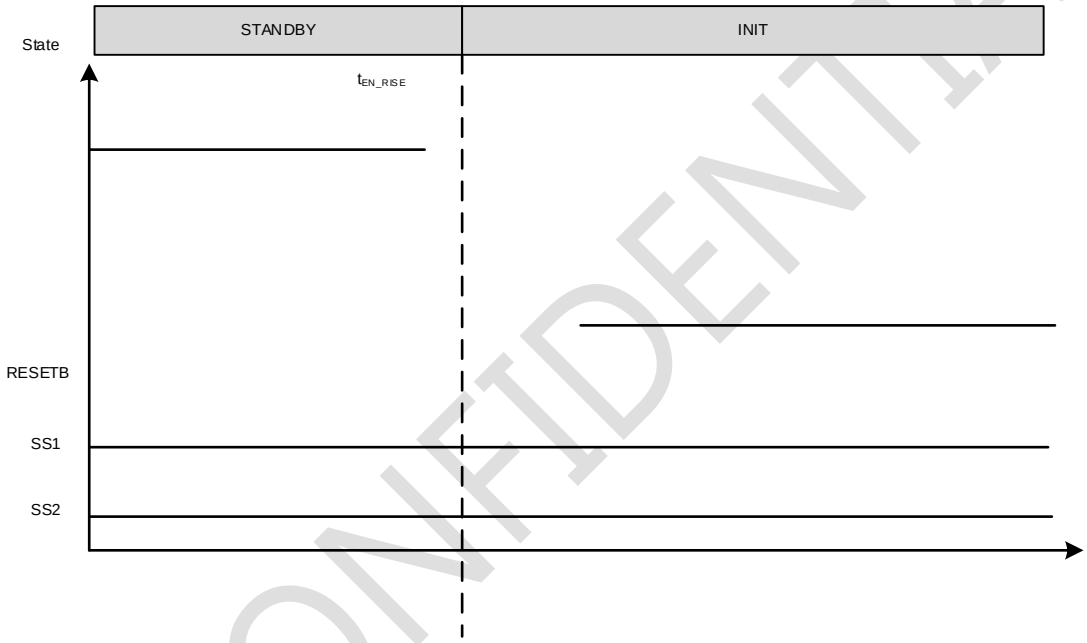
threshold

before the transition delay timer t_{TR_DEL} has expired.

7.3.7 STANDBY INIT State

Prerequisites:
• none
Triggering Events:
• Valid EN (edge) or WAKE (level) signal.
• Wake-up timer expired, if enabled
Exceptions:
• none



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• FAILSAFE timer has expired.

Triggering Events:

• Self triggered transition after the prerequisite is fulfilled.
• Valid EN (edge) or WAKE (level) signal (only needed if exception true)

Exceptions:

• In case the FAILSAFE is entered three times in a row with the same failure the self-triggered transition is blocked.

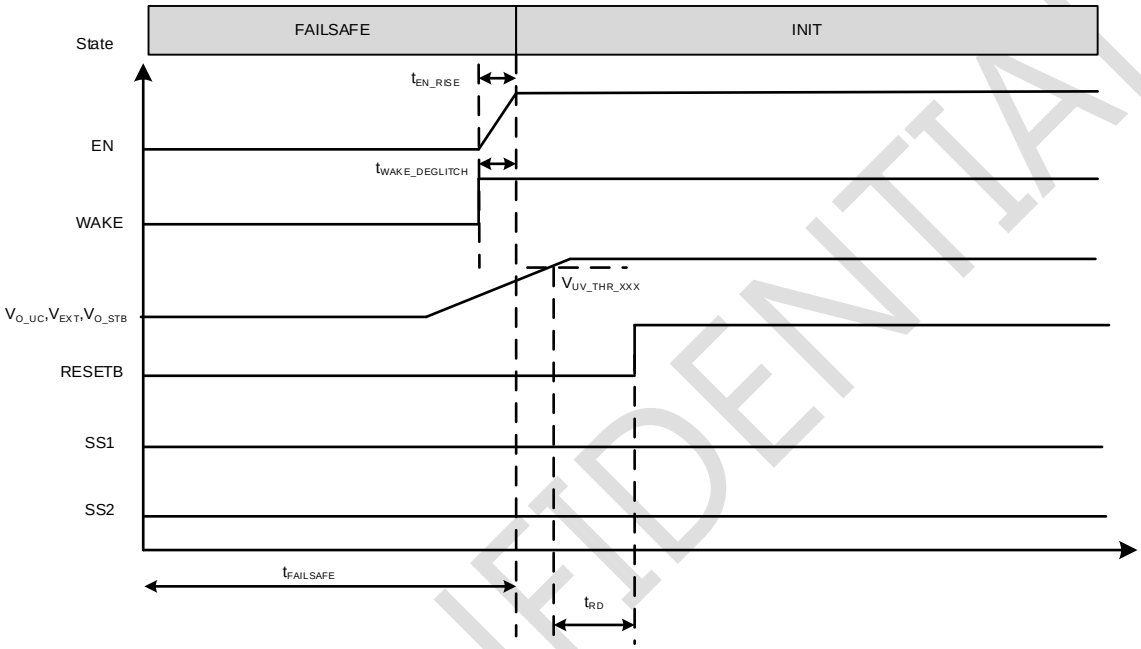

Figure 31. Transition from FAILSAFE to INIT state

• The device transition from FAILSAFE state to INIT state happens earliest after the minimum FAILSAFE time $t_{FAILSAFE}$ which is 20 ms for all failures except a thermal shutdown. In case of a thermal shutdown the minimum FAILSAFE time $t_{FAILSAFE\_TSD}$ is 1s. A command to transition before the minimum FAILSAFE time $t_{FAILSAFE}$ has expired, will not be executed.
• After entering INIT state the voltage regulators will ramp up according to the power sequencing. V_{O_UC}, V_{EXT} or V_{O_STB} (according to the previous configuration) crosses the related under voltage reset threshold $V_{UV\_THR\_XXX}$ on the way up.
• After the power on reset delay time has expired the reset (RESETB) is set to HIGH.
• The device needs to be configured and initiated. All settings done in the configuration registers before the device went into FAILSAFE state are lost, except the configuration of the LDO_STB (**RSYSPCFG0**) and the reset delay time (**DEVCFG1**).
• The safe state signal SS1 and SS2 are LOW in FAILSAFE state and will be LOW in INIT state

7.4 Reaction on detected faults

Errors are classified according to their severity into 4 different error classes:
• Stay in Current State - Failures affecting peripherals without direct risk for the microcontroller, that are indicated by an interrupt to allow analysis by the microcontroller without changing the state.
• Move to INIT - Medium severity errors that brings the device back to INIT state and generate a reset for the microcontroller.
• Move to FAILSAFE - Critical error with high risk of damaging the microcontroller.
• Move to POWERDOWN - Most critical error with high risk of damaging ourself plus the microcontroller

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Description:
• The device transition from INIT to INIT state (or stays in INIT state) for the first time is issuing a “soft reset”. Pin RESETB

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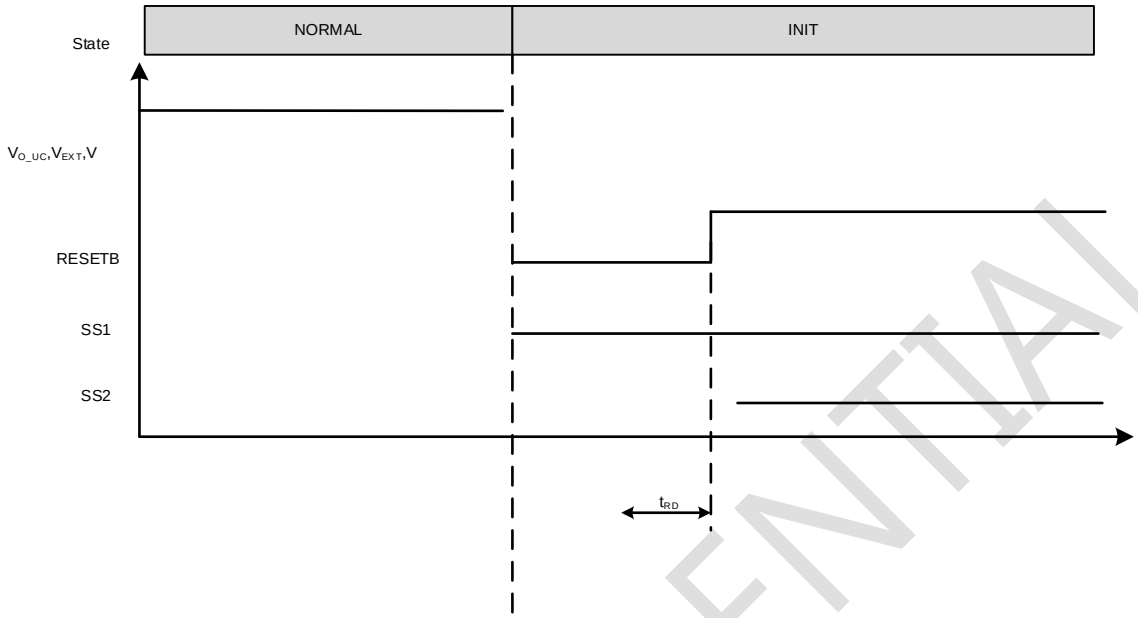

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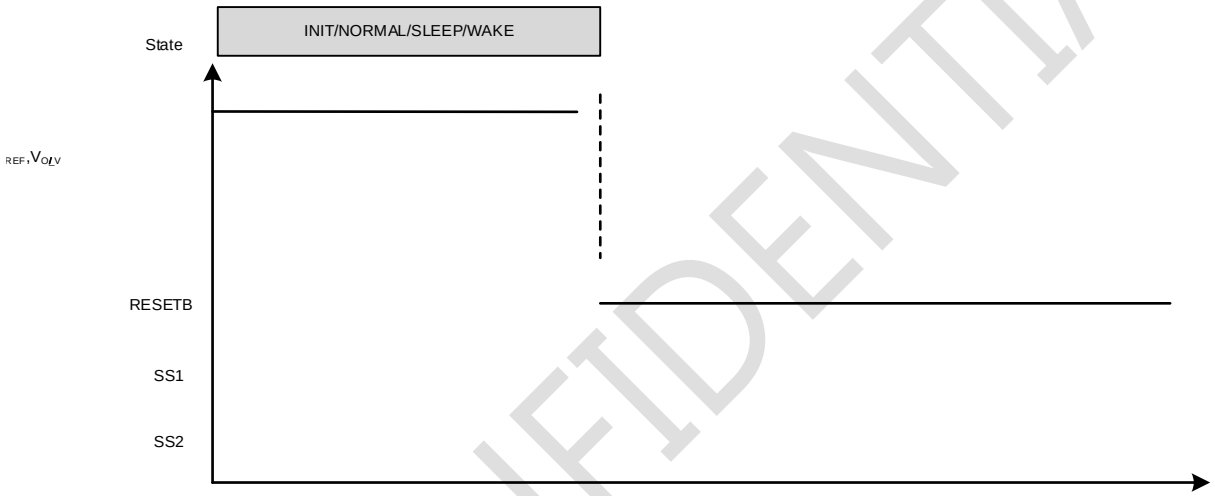
Description:
• The detection of an over voltage of the preregulator voltage VO_BK1 VO_UC, VO_STB, VEXT or VO_VREF as shown in the figure will initiate the transition from INIT/NORMAL/SLEEP/WAKE/STANDBY state to FAILSAFE state.
• Pin RESETB will be pulled to LOW as soon as the over voltage event is detected (at one or more of the regulators mentioned above - whichever is the first).
• All regulators will be switched off, when the device turns from current state into FAILSAFE state, regardless if they are in over voltage condition or not.
• Out of NORMAL state the safe state signals SS1 and SS2 will be pulled to LOW immediately with pin RESETB her state the safe state signals SS1 and SS2 are LOW and will stay low.



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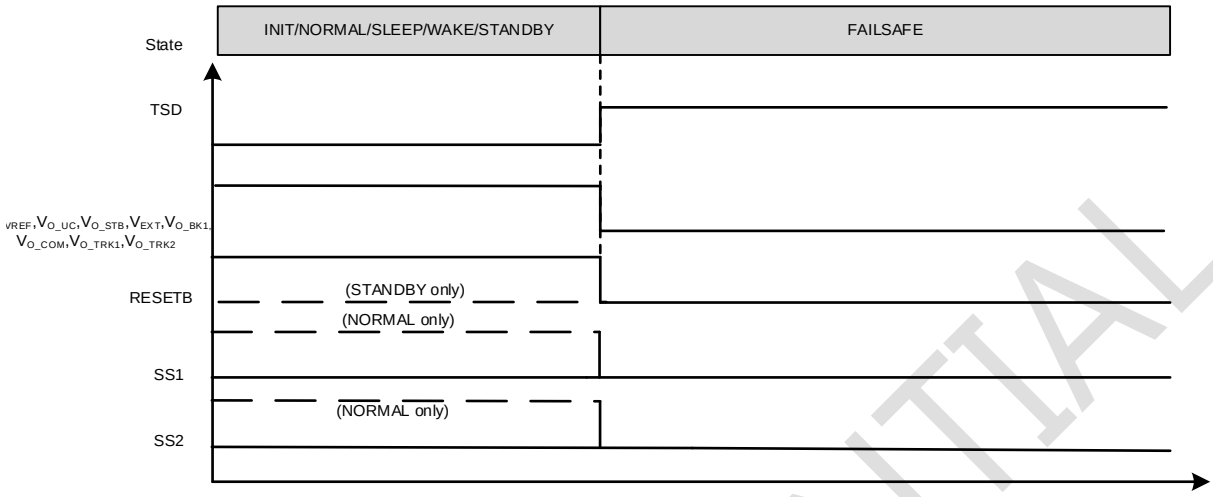

Figure 39. Transition into FAILSAFE state due to TSD fault

7.4.3 POWEROFF Events

The following failures/event will bring the device always with highest priority to POWERDOWN state:

- V_{SUP} below V_{SUP_UVLO}-$V_{SUP\_UVLO\_HYS}$ when decreasing
- Detection of over- or under voltage on internal supplies

7.5 Built In Self Test (BIST) Features

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fixed sequence of comi6e i1i1nci1i1nci16 8.5ic ccnc.1 (c)-8.1 (i1)2 ci1comncx (om)-24a (i1)-24e (nc)-8 d b.6 3.-8 y Tc 0 Tw 9.9

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• **SYSFAIL** : 00000100b (04h)
• **MONSF1** : 00101111b (2Fh)
• **MONSF2** : 00001110b (0Eh)
• **MONSF3** : 11000001b (C1h)
• Start of the test by **ABIST_CTRL0** : 00000011b (03h)
Interrupt (INTB) related:
• **IF** : 01001000b (48h)
• **INITERR** : 00000000b (00h)
• **SYSFAIL** : 00000000b (00h)
• **MONSF1** : 11010000b (D0h)
• **MONSF2** : 11110001b (F1h)
• **MONSF3** : 00110000b (30h)
• Start of the test by **ABIST_CTRL0** : 00001011b (0Bh)
This type of ABIST can be performed in the following states of the **State Machine**: INIT, WAKE, NORMAL. If this test is run in NORMAL state on comparators contributing to the secondary safety shutdown path the device will switch low the safe state outputs SS1/2 and the **State Machine** will move to WAKE state, without triggering a reset. It has to be considered that testing the complete monitoring chain till the respective output (SS1/2 or INTB) in this way will cover only the first comparator in the sequence, as this one will trigger the output reaction.
If this test is run in INIT or WAKE state, contribution to activation of the secondary safety shutdown path cannot be tested. The system is in a safe state already and the secondary safety shutdown path is already activated. In any way the proper behavior of the secondary shutdown path as well as the interrupt signal needs to be checked by the microcontroller.

7.5.2.5 Testing the complete monitoring chain (comparators, deglitching and output)

The testing of the complete monitoring chain from the comparator till the respective output function has to be divided into the two functions available in SCT61480S. First the secondary safety shutdown path called SS1/2 for severe microcontroller related failure events and secondly the interrupt function INTB for peripheral related failure events in terms of voltage and current monitoring.
• **Testing the activation of the secondary safety shutdown path:**
To test the activation of the secondary safety shutdown path, the device has to be brought into NORMAL state. The
-activated successfully (SS1/2 high).
Once in NORMAL state a single comparator contributing to the secondary safety shutdown path shall be selected. A single bit ('x') has to be set for a corresponding comparator in registers **ABIST_SELECT0** (00x0xxxxb), **ABIST_SELECT1** (0000xxx0b) or **ABIST_SELECT2** (xx00000xb). A randomized selection by the microcontroller ensures maximum coverage of the contributions to the secondary safety shutdown path. Then a single comparator ABIST operation on the full path of the secondary safety shutdown path needs to be started (register **ABIST_CTRL0**: 00000111b (07h)). Upon completion of the requested ABIST operation the device will autonomously move into WAKE state and an interrupt event is generated. The interrupt event will indicate the completion of the ABIST (**IF**.**ABIST**). Furthermore the respective monitoring failure flag for the selected comparator will be set (either **INITERR**.**VMONF** for "**Move to INIT State**" failures or **SYSFAIL**.**VMONF** for "**Move to FAILSAFE State**" failures) which has to be checked and cleared by the microcontroller.
The secondary safety shutdown path shall be
activation of the secondary safety shutdown path. If SS2 delay is enabled, this delay will be applied when the ABIST operation is performed, i.e. the activation of the shutdown path connected to SS2 will be delayed according to the programmed value for failure cases not leading to FAILSAFE.
ABIST_CTRL0.**STATUS**), the
respective monitoring status flag (**MONSF1**, **MONSF2** or **MONSF3**) to be set according to the previous selection and **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2** bits to be cleared.
Furthermore, the microcontroller has to proceed with the following steps to check the safe state control and the safe state outputs:
• Check that the secondary safety shutdown path has been activated successfully (SS1/2 low)
• Enable overvoltage trigger of the safe state control (set **ABIST_CTRL1**.**OV_TRIG**)
activated successfully (SS1/2 low)
• Select generation of valid toggling signal for the safe state control (set **ABIST_CTRL1**.**ABIST_CLK_EN**)

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• De-select generation of toggling signal for the safe state control (reset **ABIST_CTRL1**.**ABIST_CLK_EN**)

• Disable overvoltage trigger of the safe state control (set **ABIST_CTRL1**.**OV_TRIG**)

Afterwards a test of all comparators which contribute to the activation of the secondary safety shutdown path shall be configured and started.

• Testing the generation of an interrupt event:

The test of the generation of an interrupt event can be done in the states INIT, NORMAL and WAKE state. Even though it is recommended to have the application in safe state (INIT or WAKE state).

For this test first a single comparator contributing to the interrupt function shall be selected. A single bit ('x') has to be set for a corresponding comparator in registers **ABIST_SELECT0** (xx0x0000b), **ABIST_SELECT1** (xxxx000xb) or **ABIST_SELECT2** (00xx0000b). A randomized selection by the microcontroller ensures maximum coverage of the contributions to the interrupt function. Then a single comparator ABIST operation on the full path of the interrupt needs to be started (register **ABIST_CTRL0**: 00001111b (0Fh)). The artificial failure, triggered by the ABIST controller, on the selected comparator will generate an interrupt (INTB) event. It is the responsibility of the to check the generation of this interrupt event on the triggered failure. As this is a test of the generation of an interrupt based on a failure event, there is no dedicated ABIST completion event, nor the **ABIST** bit in the interrupt flags will be set. Accordingly it is recommended to store the information about the started ABIST in the firmware.

After the interrupt has been generated the interrupt flag register shall be checked for the monitoring bit (**IF**.**MON**) set and the ABIST completion bit (**IF**.**ABIST**) not set.

ABIST_CTRL0.**STATUS**), the respective monitoring status flag (**MONSF1**, **MONSF2** or **MONSF3**) to be set according to the previous selection and **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2** bits to be cleared.

Afterwards a test of all comparators which contribute to the interrupt generation shall be configured and started.

7.5.2.6 Abort conditions for ABIST operation

In case of an severe monitoring failure event (contribution to the secondary safety shutdown path) detected on a not selected comparator1) or a severe failure event not related to the voltage or bias current monitoring function during the proceeding of an ABIST operation on the comparators only (**ABIST_CTRL0**.**PATH** not set), the device will react as it is supposed to do in normal operation. Accordingly the monitoring, reset and safe state control are reacting. Bringing the device into safe state and trigger the **State Machine** to move into FAILSAFE or INIT state. The ABIST is aborted in this case.

In case of an ABIST operation on the full path (**ABIST_CTRL0**.**PATH** set) the comparators for voltage and bias current monitoring are blind for the time of the ABIST operation. Therefore it is recommended to do the test in safe state unless it is needed to start the test in NORMAL state (e.g. test of activation of secondary safety shutdown path). Severe failure events not related to the voltage and bias current monitoring will trigger the same device reaction as in usual condtion. Bringing the device into safe state and trigger the **State Machine** to move into FAILSAFE or INIT state. The ABIST is aborted in this case.

This ABIST abort will be recorded in the register **SYSFAIL**.**ABISTERR**. The artificial failure events, that have been generated until the abort of the ABIST due to the detected real failure, will be stored as well in the monitoring registers.

7.6 Microcontroller Programming Support

The device offers a microcontroller programming support feature, that can be used to avoid periodic reset triggering due to missing triggering of the window watchdog and error monitoring within the INIT timer. The activation of the microcontroller programming support feature shall be done by pulling the PROG pin to 5 V. The voltage shall be provided earliest with the enabling of the voltage reference. Therefore it would be one option to connect the PROG pin to the output VO_VREF during microcontroller programming.

The active microcontroller programming support feature includes the following changes to the normal operation of the device:

The INIT timer will be stopped.

The contribution of the window watchdog failure counter overflow to the reset will be blocked.

The contribution of the functional watchdog failure counter overflow to the reset will be blocked.

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The contribution of the error monitoring to the reset will be blocked.

As only the contribution of the watchdogs and the error monitoring to the reset function is blocked/disconnected, the state machine and safe state control function are not affected. Accordingly an overflow of the window or functional watchdog failure counter will trigger a “Move to INIT” event, but without issuing a reset of the microcontroller.

The microcontroller programming support feature offers as well the possibility to move the device to any other state according to the state machine. E.g. in case PROG pin is high in NORMAL and there is a watchdog error counter overflow the device would move into INIT without issuing a reset.

8 Safe State Control Function

8.1 Introduction

The safe state control monitors safety related signals and controls the safe state signals SS1 and SS2.

The following description summarizes the contributors to the safe state control function and the possibilities to adjust them.

Principle of operation:

The safe state control function monitors the following inputs:

• Result of the Error Monitoring. “Error”-signal at pin ERRIN is expected to be a toggling signal. A permanent low or high signal will be detected as an error.

• Over and under voltage of the micro processor related regulators

• Result of Window Watchdog Failure Counter Threshold Comparator. Whether threshold ΣWWO for “Invalid window watchdog triggering” has been exceeded.

• Result of Functional Watchdog Failure Counter Threshold Comparator: Whether threshold ΣFWO for “Invalid functional watchdog triggering” has been exceeded.

• Thermal shutdown signal (TSD) for relevant events moving the device into FAILSAFE state.

• Internal clock

• SPI state transition request. A valid GoToNORMAL command triggers the signals SS1/2 to switch high in case the other boundary conditions are fulfilled. Moving the device out of NORMAL state by SPI command will switch the signals SS1 and 2 (optionally delayed by t_{SS_DLY}) to low.

The following parameters of the safe state control function are programmable via SPI, this settings can be done during INIT, NORMAL, SLEEP and WAKE state, WWD and FWD configuration and error pin configuration including disabling of individual functionality via protected register:

• Number of invalid watchdog triggers, that lead to activating SS1 and SS2: There are two watchdog trigger failure counters implemented, one for the window watchdog the other for the functional watchdog. Every counter increments by two at every invalid watchdog triggering and decrements by one at every valid watchdog triggering. (valid and invalid triggering is described in chapter functional and window watchdog). An incrementing change is indicated by an interrupt. A decrementing change is not indicated by an interrupt. The thresholds can be programmed by SPI command for each counter individually. This function might be used to test the watchdog function.

• Immediate reaction or recovery delay reaction, only related to input signal ERR: This parameter determines whether the safe state control will immediately react to an error indicated by SMU or react after a certain delay, if the error indication is still present. In recovery delay reaction the safe state control will generate an interrupt and start the programmed recovery delay time. If within this time the error should disappear (means the error signal should toggle again, before the recovery delay time has ended), the safe state control will keep the safe state output SS1/2 high. If within this time the error signal should not disappear and maintain the error indication (means the error signal should not toggle again, before the recovery delay time has ended), the safe state control will activate the safe state signals SS1 and SS2 after the recovery delay time has ended.

Immediate reaction means reaction after signal detection delay time.

• Recovery delay time t_{REC}, only related to input signal ERR: An error (violation of valid ERR signal) has to be longer than this delay time to lead to activating the safe state signals SS1 and SS2. This delay time is only active if recovery delay time mode was selected.

• Delay time t_{SS_DLY} between safe state signal 1 and safe state signal 2

The safe state function offers two output signals, both of them as output stages to drive external switches (additional

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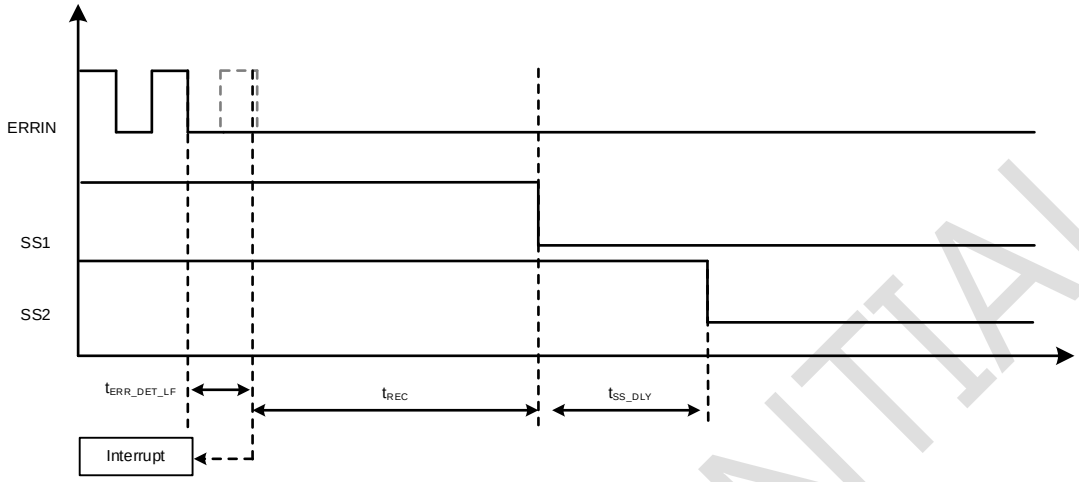

Figure 46. Flow diagram reaction on SMU signal, error longer than recovery delay time

• ERRIN signal frequency too high

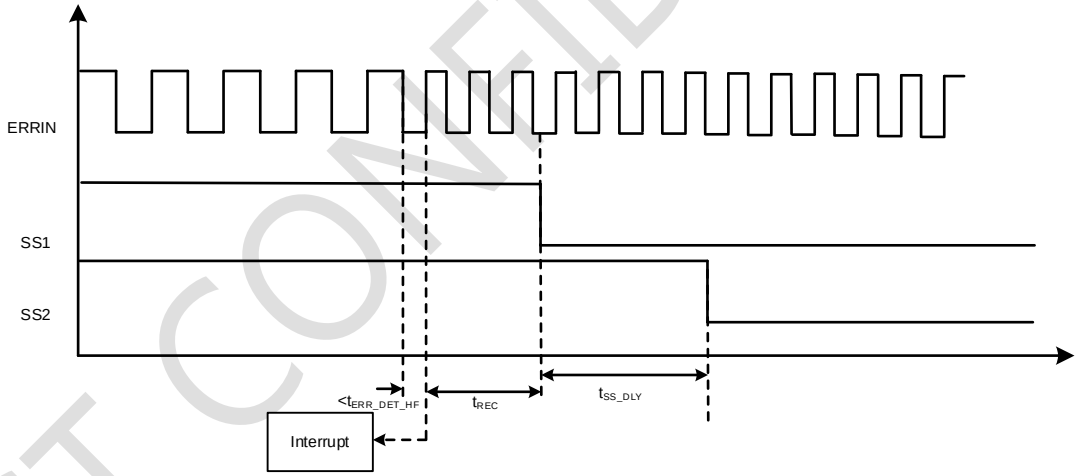

Figure 47. Flow diagram reaction on SMU signal, error longer than recovery delay time (ERRIN signal frequency too high)

• ERRIN remains low or high and error shorter than recovery delay time

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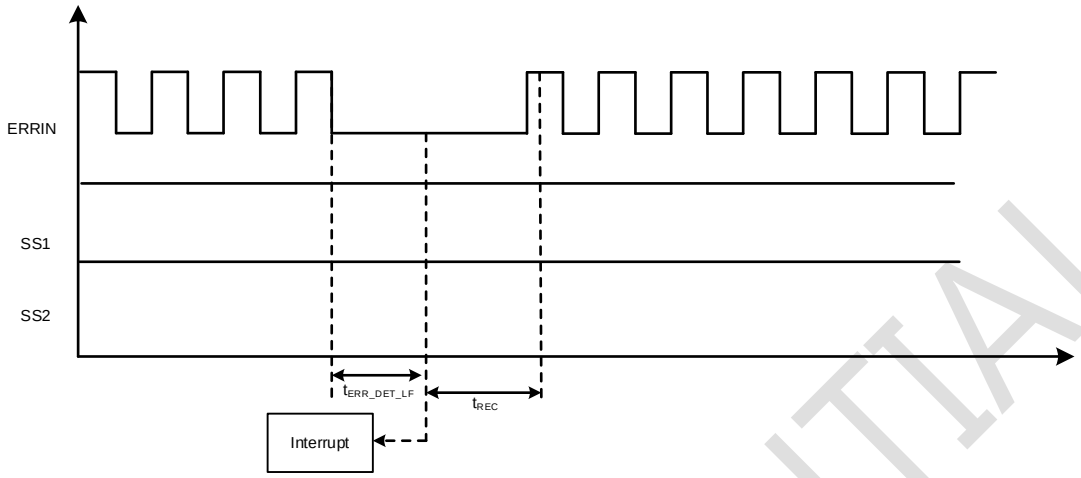

Figure 48. Flow diagram reaction on SMU signal, error shorter than recovery delay time

• ERRIN signal frequency too high and error shorter than recovery delay time

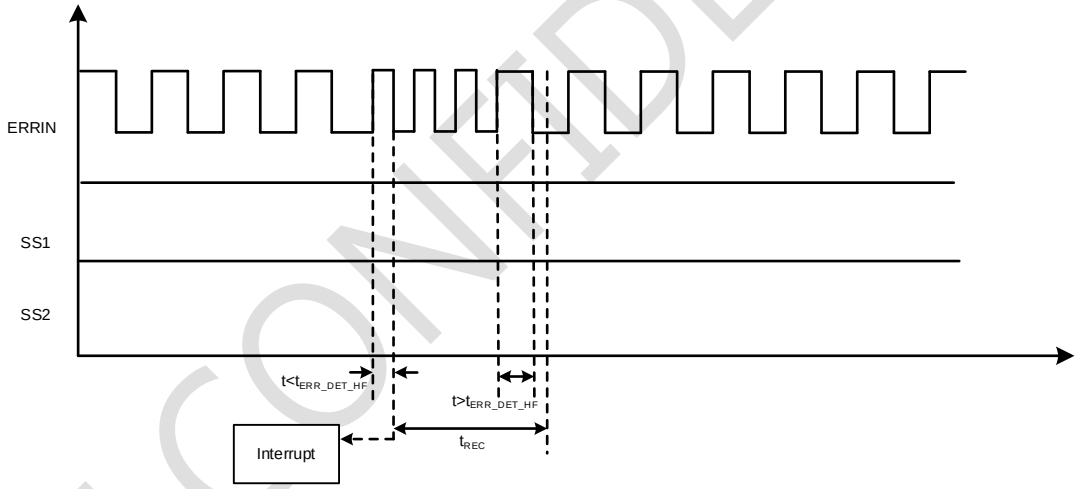

Figure 49. Flow diagram reaction on SMU signal, error shorter than recovery delay time (ERRIN signal frequency too high)

8.3 Reaction on Error Triggered State Transitions

• Soft reset

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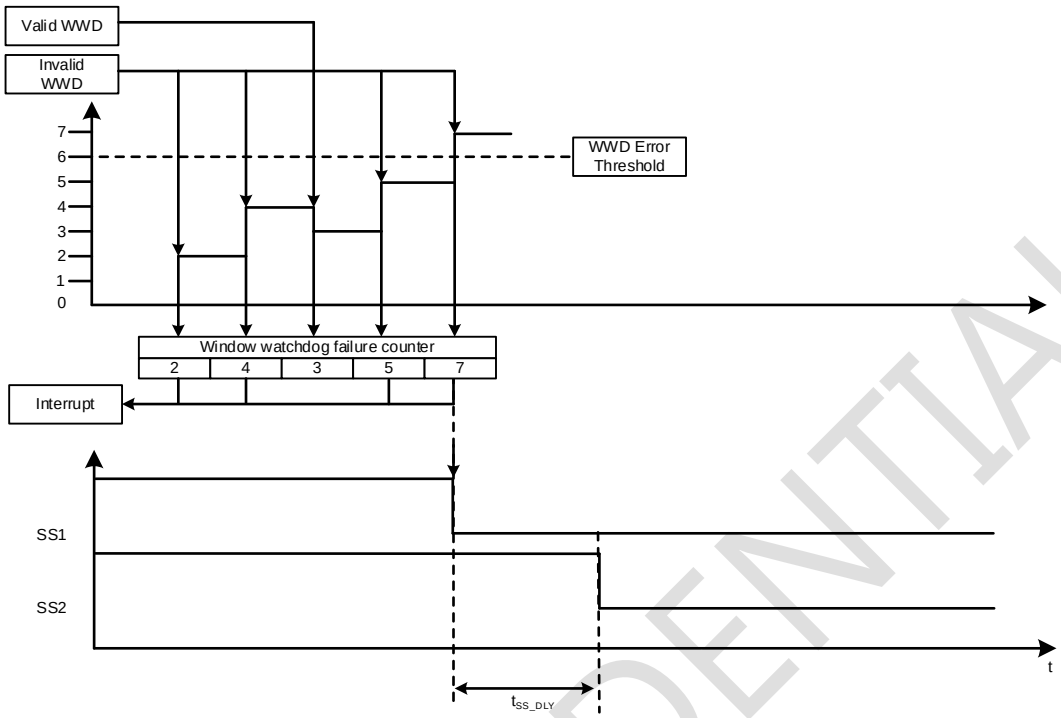

Figure 52. Flow diagram reaction on WWO

8.5 Reaction on Functional Watchdog Output (FWO)

The SCT61480S has an implemented functional watchdog failure counter (**FWDSTAT1**.**FWDECNT**). The counter increments by two at every invalid functional watchdog triggering and decrements by one at every valid functional watchdog triggering. (For specification of valid and invalid triggering please refer to chapter functional and window watchdog).

The status of the functional watchdog failure counter is written in the so called functional watchdog status counter. Any incrementation of the functional watchdog status counter is indicated by an interrupt. Any decrementation of the functional watchdog status counter is not indicated by an interrupt. The content of the functional watchdog status counter cannot be less than zero.

The threshold for activating the safe state signals SS1 and SS2 FWO can be changed in INIT, NORMAL and WAKE state. (**WDCFG1**.**FWDETHR**)

The content of the status counter will be compared to the programmed threshold FWO (**RWDCFG1**.**FWDETHR**). If the content of the status counter is equal or higher than FWO, the safe state signals SS1 and SS2 will be activated (low).

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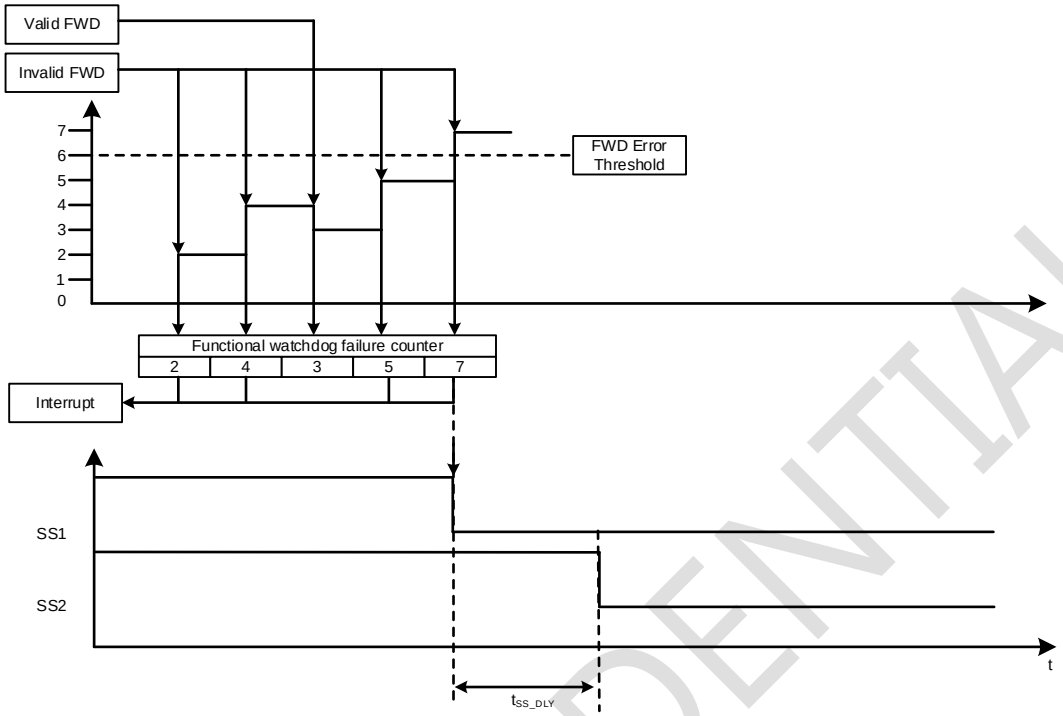

Figure 53. Flow diagram reaction on FWO

8.6 Reaction on Thermal Shutdown (TSD)

The thermal shutdown (TSD) indicates temperature overstress: on the chip: As a consequence all pre and post regulators will be shut down immediately.

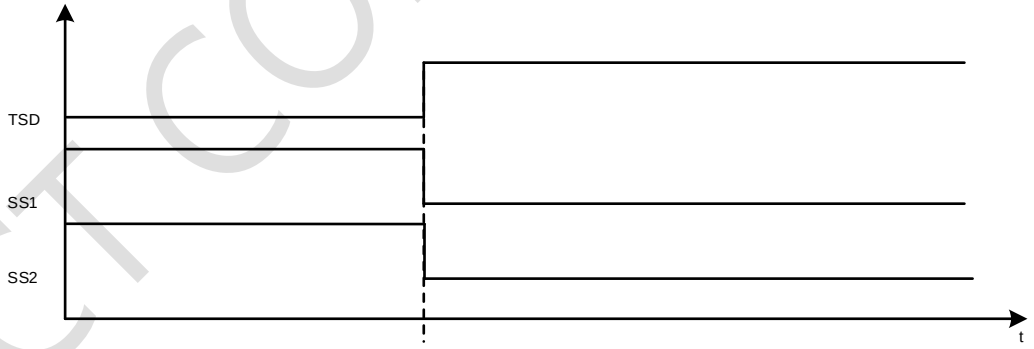

Figure 54. Flow diagram reaction on TSD

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and will be taken over with the rising edge of the CS at the end of the second command.
In case of an invalid request (wrong sequence or DEVCTRLN not inverted to DEVCTRL) it will be rejected, an interrupt is generated and the corresponding status flag (**NO_OP**) is set. Incase of an invalid state transition request, the request is ignored without issuing an interrupt.

10 Interrupt Generation

A dedicated interrupt generation block is implemented which is handling requests from independent sources to generate an interrupt. The different requesters are as follows:
• State machine in case:
– A requested state transition has not been performed successfully, e.g. SLEEP state could not be entered because

– A requested

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After an interrupt has been detected by an uC, the recommended interrupt service routine would need to perform the following tasks via SPI:
1. Read interrupt flag register (**IF**)
2. Read status flag register(s) based on information from first read
3. Take the proper action based on interrupt flag(s) and status flag(s)
4. Write back the status flag register(s) to clear particular status flag(s)
5. Write back the interrupt flag register (**IF**) with the previously read value to clear
6. Recommended: Read interrupt flag register (**IF**) again to check for occurrence of another interrupt event. In case step back to 2).
7. Writing back the interrupt register (**IF**) will release the interrupt line INTB if all bits are cleared (interrupt timing requirements will be fulfilled).

An interrupt is only generated after the reset signal to the uC has been released. An interrupt event which occurred while the reset line for the uC is still active is not signaled at the interrupt line but the particular status bit for this event is set.
Details about the timing of the interrupt line are depicted in the following figure:

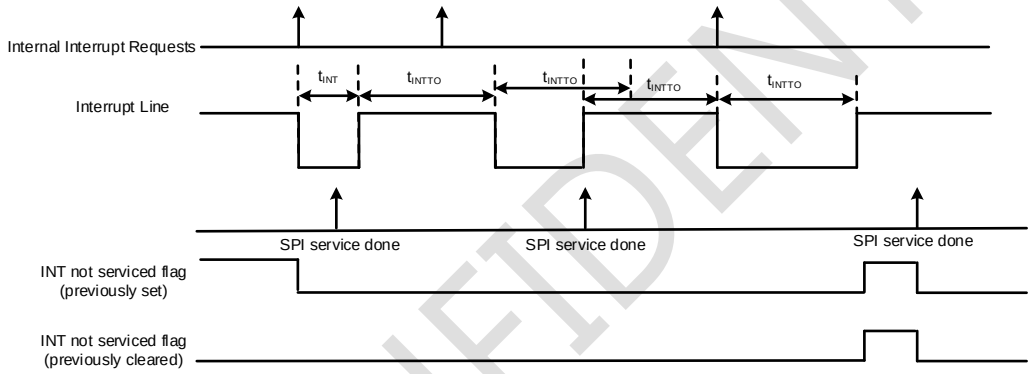

Figure 56. Interrupt timing

Details about the system behavior in case not all interrupt status flags have been cleared are depicted in the following figure:

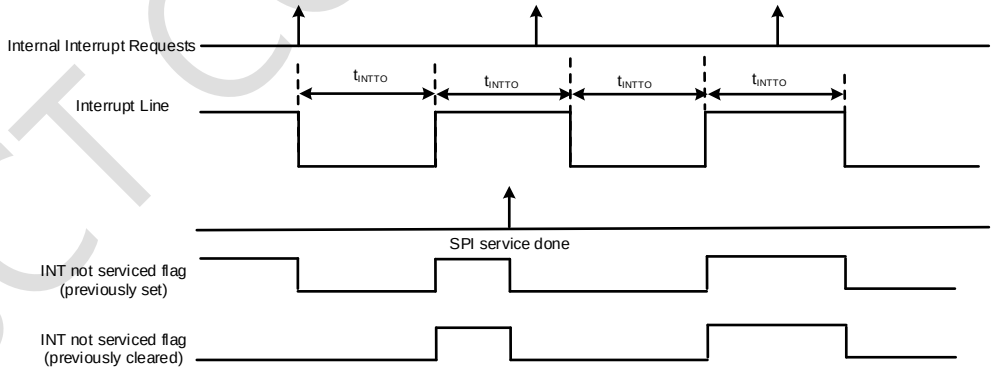

Figure 57. Interrupt timing without service in time

An interrupt is always generated if an internal status flag is set, irrespective of the current state of this status flag. For example, if a parity error on SPI communication is detected for the first time, the flag **SPISF.PARE** is set and an interrupt is generated. This flag will also set the corresponding SPI interrupt flag (**IF.SPI**). If the flag **IF.SPI** is not cleared, but a second SPI parity error occurs, a new interrupt will be generated regardless. The timings shown in

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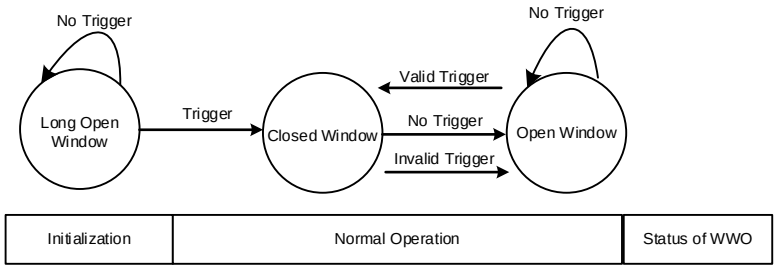

Figure 59. Watchdog state diagram

Window watchdog trigger pin WDI

The watchdog input pin WDI has an integrated pull-down current I_{WDI_PULL}. The watchdog input WDI can transition to high within the "Closed Window" or during the following "Open Window".

Valid Trigger Signal at WDI

Watchdog input WDI is periodically sampled with a period of t_{WD_SAMPLE}. A valid trigger signal is a falling edge from V_{WDI_H} to V_{WDI_L}. To improve immunity against noise or glitches on the WDI input, at least two high samples followed by two low samples are required for a valid trigger signal, the valid triggering is considered with the second consecutive sampling point measuring low signal. For example, if the first three samples (two high one low) of the trigger pulse at pin WDI are inside the “Closed Window” and only the fourth sample (the second low sample) is taken in the “Open Window” then the watchdog output WWO will indicate “valid WWD triggering”.

Invalid Triggering at WDI

No trigger signal detected during the "Open Window" or a trigger signal detected during the "Closed Window", is considered invalid triggering. Watchdog output WDO indicates “invalid triggering” immediately after no valid trigger during the "Open Window" or immediately if a trigger signal is detected during the "Closed Window".

11.2.2 Timing Diagrams

Correct triggering

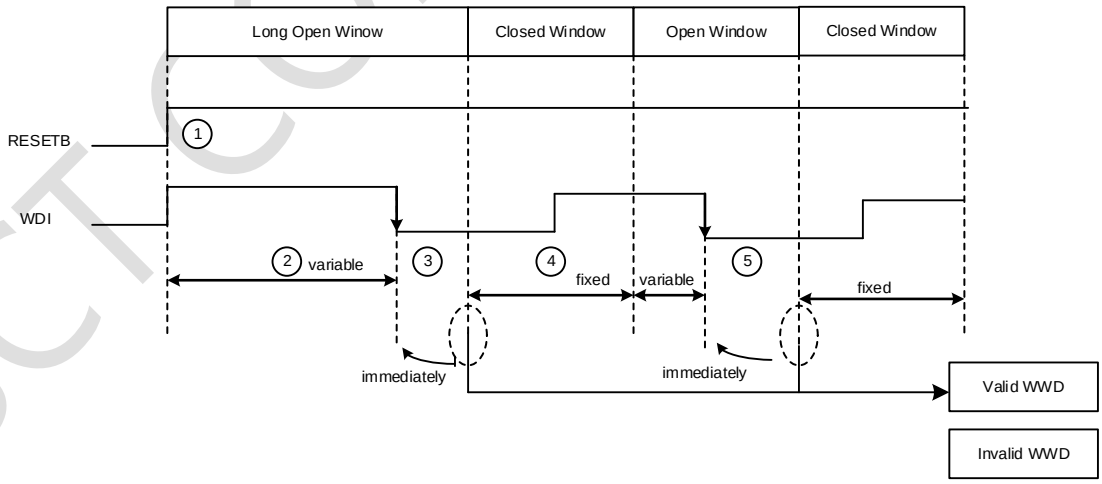

Figure 60. Normal operation: Correct triggering

1. The “Long Open Window” starts in INIT state if the reset output of RESETB (monitoring the microcontroller related voltages) turned high. In case the window watchdog was deactivated in SLEEP, the first Open Window starts with the transition from SLEEP state to WAKE state which is indicated by interrupt. The time of this first Open Window depends on the configured cycle time and is 600 ms (**WDCYC** = 1) or 60ms (**WDCYC** = 0)

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2. During the “Long Open Window” valid triggering of the WWD according to the configured trigger selection is expected. The maximum time of the “Long Open Window” is fixed, but it will be terminated as soon as a “Valid WWD triggering” is recognized.
3. The window watchdog will enter now the ”Closed Window”. After receiving this first valid trigger the device will be allowed to move from INIT to NORMAL state or from WAKE to NORMAL state.
4. The “Closed Window” has a fixed duration t_{WD_CW} (can be determined by SPI command). It starts right after the valid trigger signal, that closes the “Open Window” or the “Long Open Window”. During the “Closed Window” no trigger signal should be applied. A transition from low to high at the WDI pin is not detected and will not lead to a trigger event,
5. A valid trigger signal terminates the “Open Window” immediately, thus the time of the “Open Window” is variable and depending on the time the microcontrollers schedules the triggering. This is counted as a “Valid WWD triggering”

Incorrect triggering: No trigger in W1D

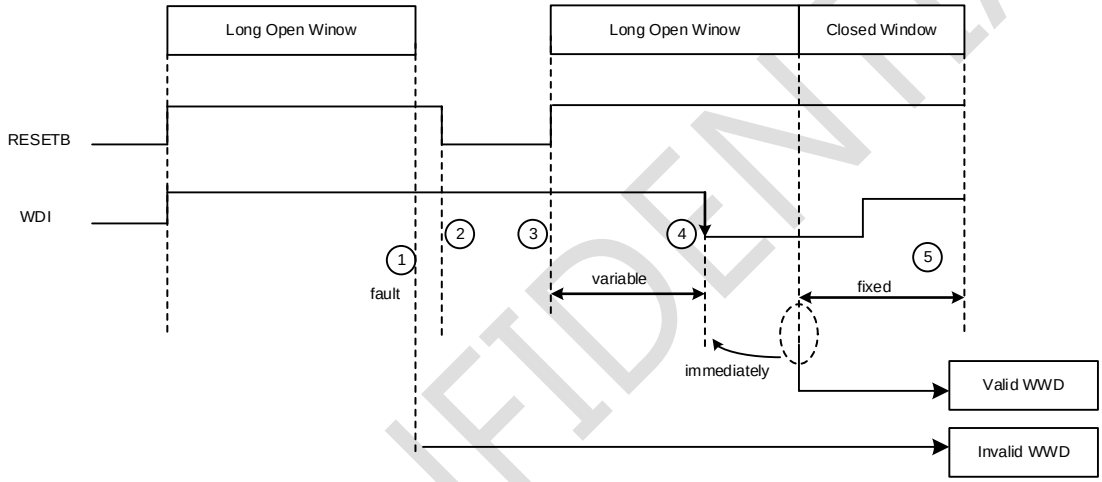

Figure 61.

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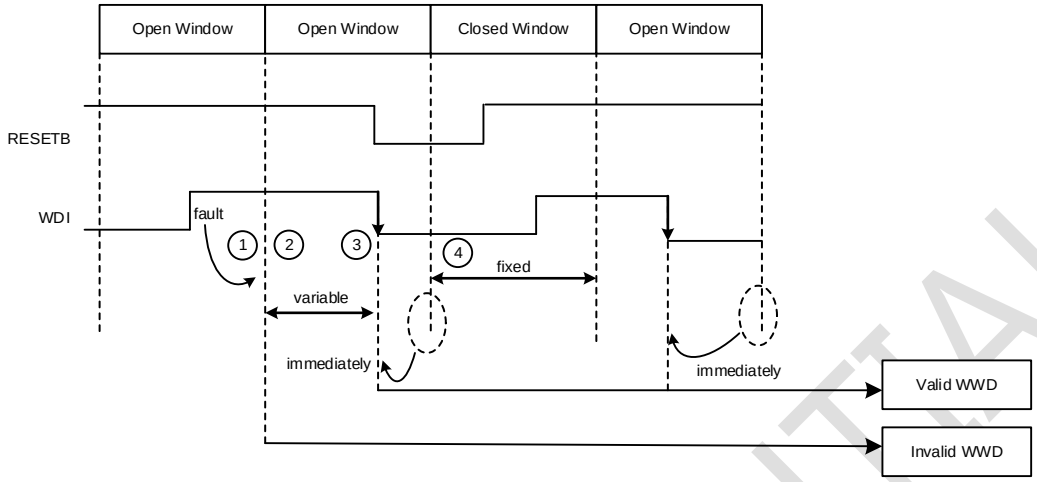

Figure 62. Fault operation: No trigger in Open Window in steady state

1. A missing valid triggering within the “Open Window” leads after the window has ended to an “Invalid WWD triggering”. This event is indicated by an interrupt, the window watchdog failure counter increases by two.
2. Having detected an “Invalid WWD triggering” the watchdog will start a new “Open Window” with duration t_{WD_OW} to give the microcontroller the chance to trigger and synchronize to the watchdog period.
3. A valid triggering terminates the “Open Window”, which makes the duration of the “Open Window” variable and depending on the triggering. This is counted as a “Valid WWD triggering” and a “Closed Window” is started.
The window watchdog failure counter will be decremented by one without an interrupt issued.
Additional informations: In case of multiple “Invalid WWD triggering” within the “Open Windows”, the window watchdog failure counter would be incremented again by two until it reaches the configured threshold. In this case a reset will be issued.
4. The following “Closed Window” lasts for the time t_{WD_CW}. Triggering within this time will be considered as an ”Invalid WWD triggering”.
The behavior of pin RESETB is depending on the value of WWO. In the example above it was assumed, that the invalid triggering will not lead to exceed the threshold WWO.

Incorrect triggering: False trigger in W1D

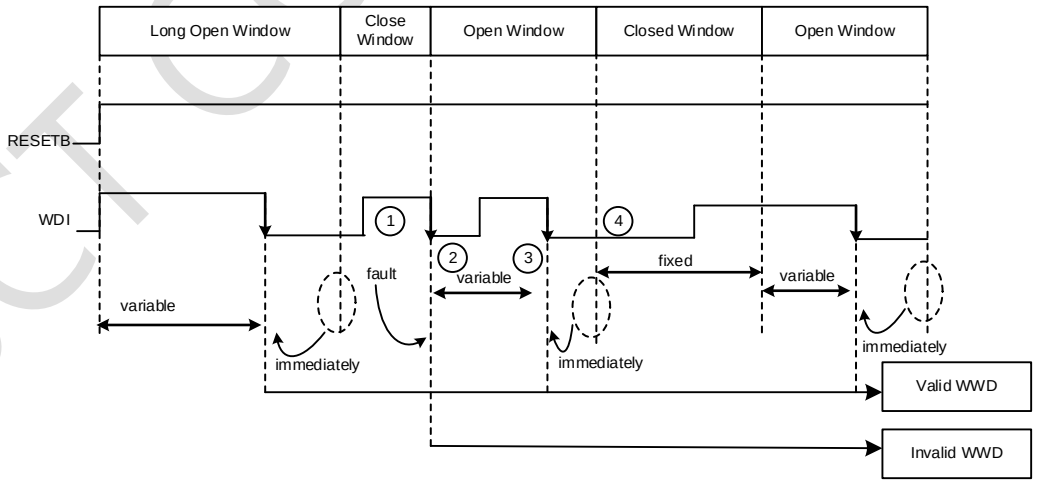

Figure 63. Fault operation: False trigger in Closed Window after initialization

1. A triggering during the “Closed Window” is indicated as “Invalid WWD triggering”. This event is indicated by an interrupt and the window watchdog failure counter increases by two.

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consists of 4 responses of 8 bits each. The four responses shall be sent before the heartbeat period has ended. The last response shall be written to the synchronized response register to reset the heartbeat counter.

Initialization

The functional watchdog is off per default when the device is powered up for the first time. It can be enabled by SPI writing to **WDCFG0**.**FWDEN**.

Configuration

The functional watchdog can be configured in INIT, NORMAL and WAKE state. “Configured” means:

• Modify the length of the heartbeat period by SPI command, depending on the needs of the application. (combination of cycle time **WDCYC** and number of cycles for heartbeat **WDHBTP**)

• The threshold for the functional watchdog failure counter overflow can defined by SPI The heartbeat period is based on the cycle time t_{CYCLE}.

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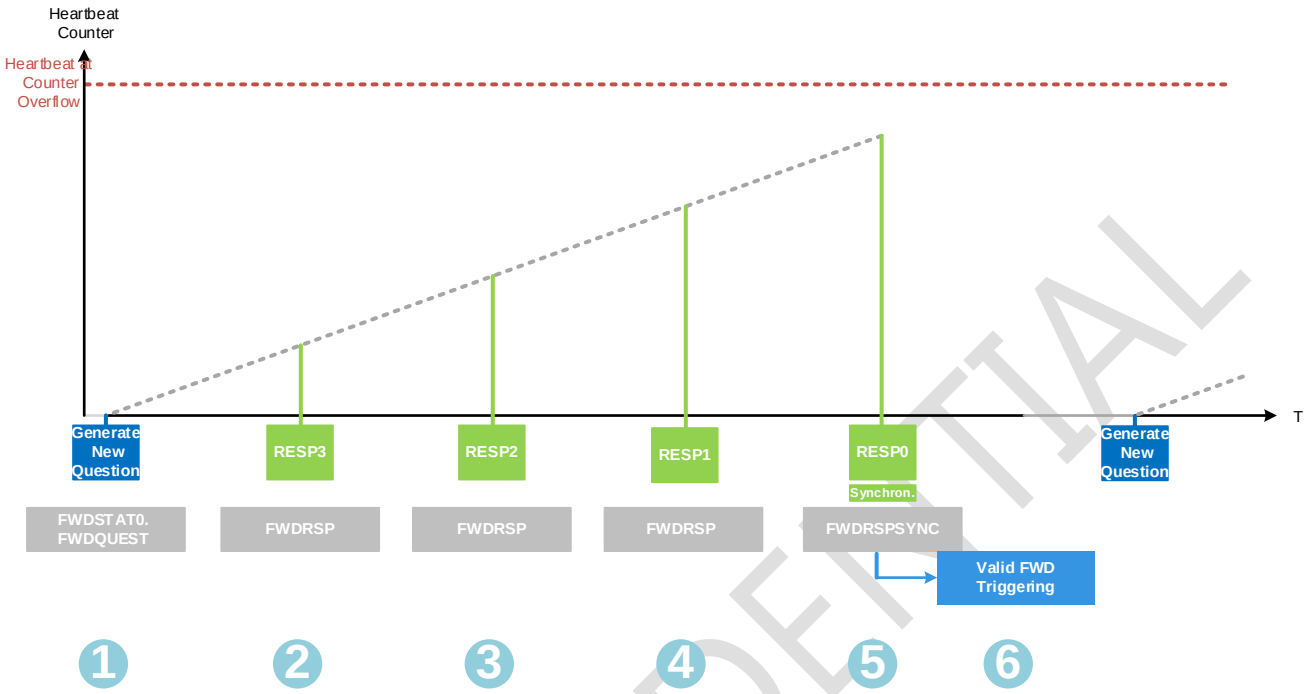

Figure 66. Normal operation: Correct triggering

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a “Valid FWD triggering” has happened before).
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. A correct response is received (RESP1)
5. A correct synchronized response is received (RESP0). All responses are correct, the sequence of responses is correct and the last synchronized response was received before the heartbeat counter overflowed. The heartbeat counter will be reset (set to zero). This is regarded as “Valid FWD triggering”, the functional watchdog error counter FWO is decremented by 1 (if the functional watchdog error counter value is higher than zero).
6. A new question is generated, in parallel the heartbeat counter starts counting up

Incorrect triggering: Synchronization is missing

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12 Typical Application

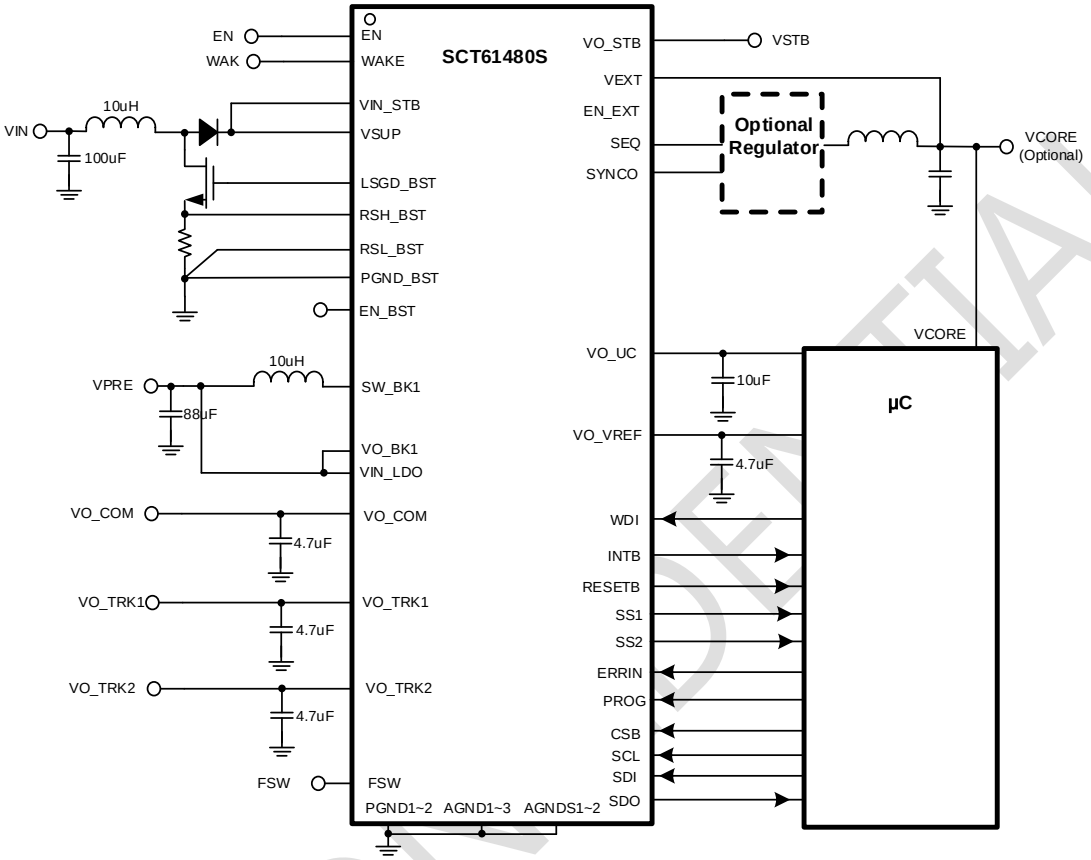

Figure 70. Application Schematics, 3V to 40V Input

Design Parameters	Example Value
Input Voltage	12V Nominal 3V to 40V
Output Voltage	VO_BK1: 5.8V VO_UC: 5V VO_STB: 5V VO_COM: 5V VO_VREF: 5V VO_TRK1/2: 5V
Maximum Output Current	VO_BK1: 1.5A VO_UC: 800mA VO_STB: 20mA VO_COM: 600mA VO_VREF: 200mA VO_TRK1/2: 200mA
Switching Frequency	400kHz/2.2MHz (selectable)

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The SCT61490S is featured with minimized external components and any feedback divider or configuration resistor could be saved. For typical application, the recommended inductance and capacitance for each power rail are listed in Table 11. Higher inductance and capacitance for lower output ripple are also acceptable.

Table 11. Recommended BOM for Typical Application

Power Rail	Switching Frequency	Inductor	Output Capacitor
VO_BK1: 5.8V	400kHz	10~22uH	10~47uF
VO_BK1: 5.8V	2.2MHz	4.7~10uH	68~100uF
VO_UC: 5V	-	-	2.2~47uF
VO_STB: 5V	-	-	1~10uF
VO_COM: 5V	-	-	1~47uF
VO_VREF: 5V	-	-	1~10uF
VO_TRK1/2: 5V	-	-	1~10uF

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12.1 Application Waveforms

V_{IN} = 12V, V_{BK1} = 5.8V, V_{UC} = 5V, V_{STB} = 5V, V_{COM} = 5V, V_{VREF} = 5V, V_{TRK12} = 5V, L1 = 10uH, T_A = 25°C, unless otherwise noted.

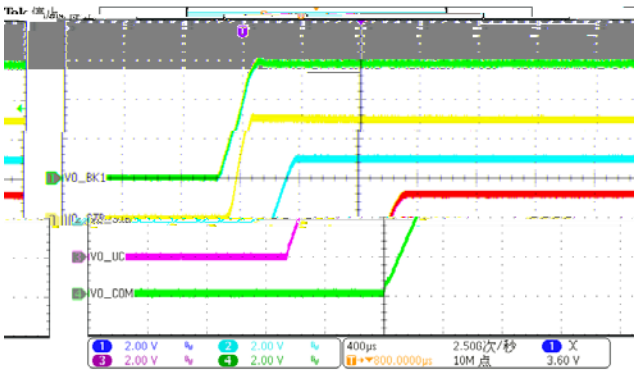

Figure 71. Power On Sequence I

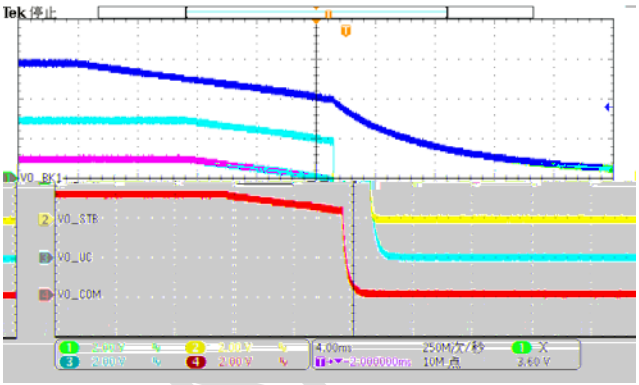

Figure 72. Power Off Sequence I

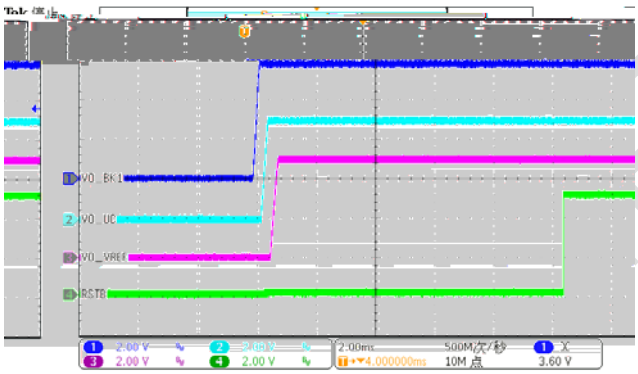

Figure 73. Power On Sequence II

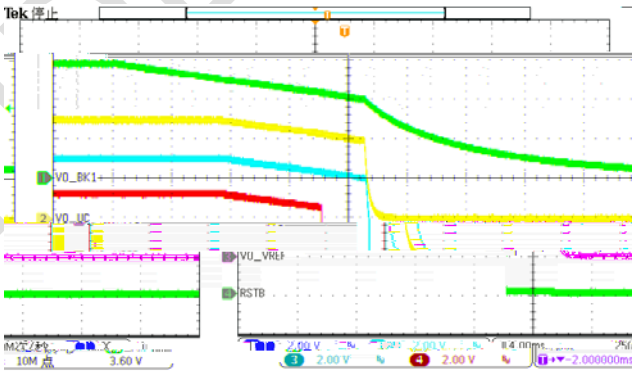

Figure 74. Power Off Sequence II

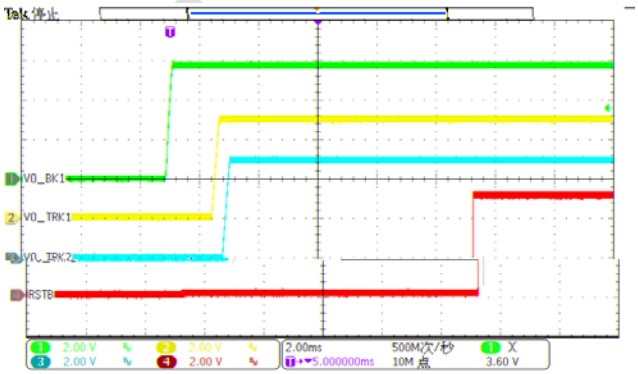

Figure 75. Power On Sequence III

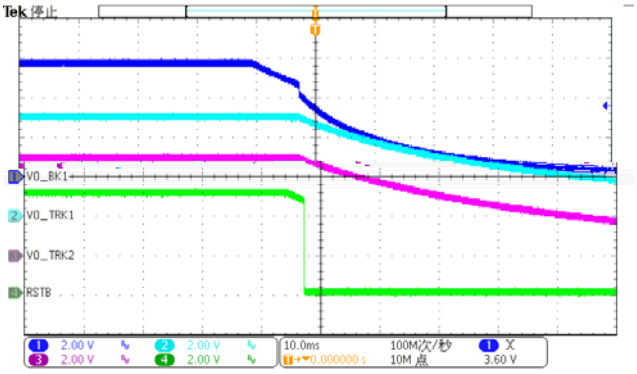

Figure 76. Power Off Sequence III

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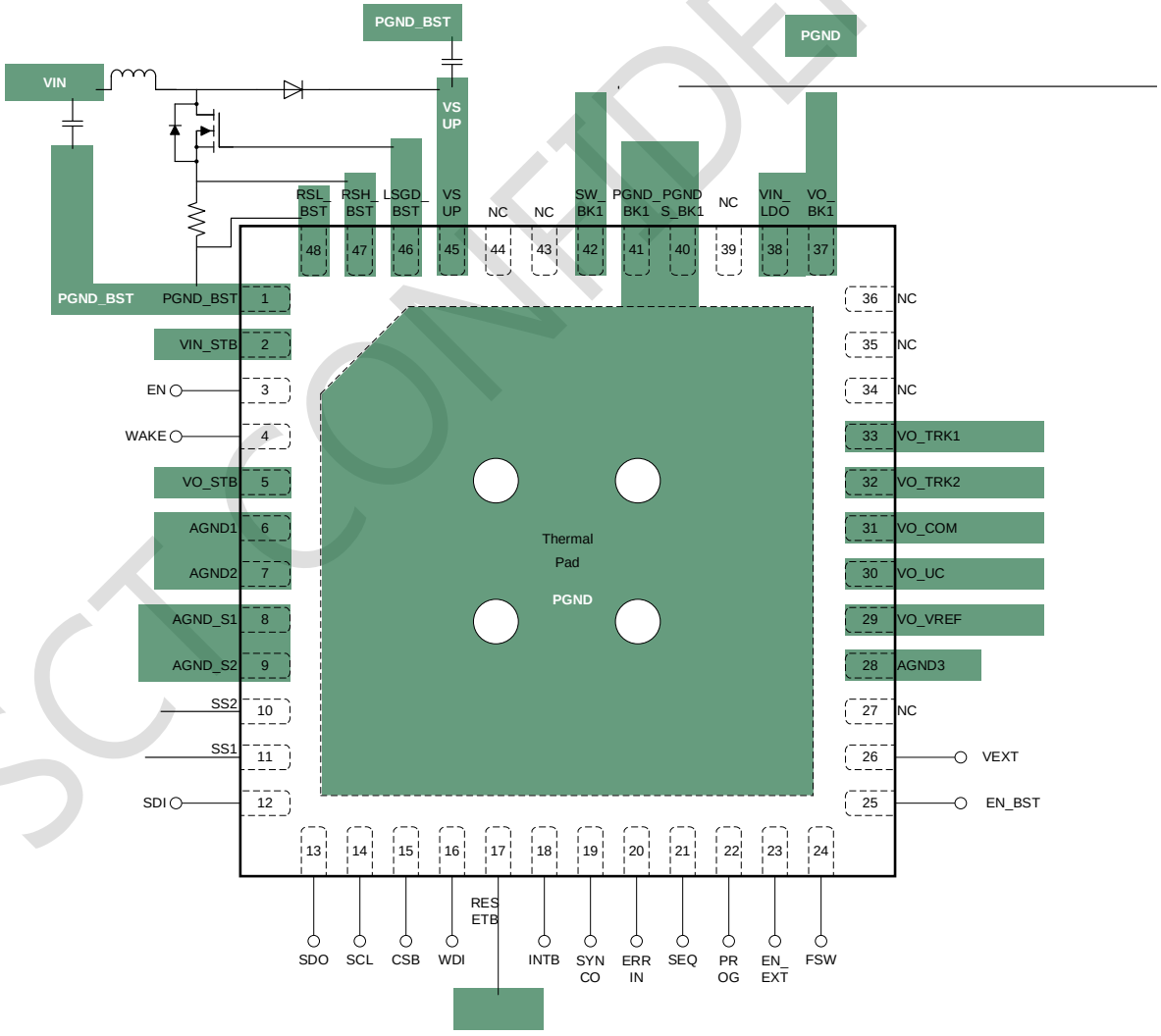
12.2 Layout Guideline

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The rule of thumb is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over-heat area.
2. Place a low ESR ceramic capacitor as close to VIN, VIN_BK2 and VIN_LDO pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.
5. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. Connect AGND to PGND plane at a single point.



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0x09	WWDCFG0	06h	R2
0x0A	WWDCFG1	0Bh	R2
0x0B	RSYSPCFG0	01h	R0
0x0C	RSYSPCFG1	00h	[7:5]: R1 [4:0]: R3
0x0D	RWDCFG0	9Bh	R3
0x0E	RWDCFG1	09h	R3
0x0F	RFWDCFG	0Bh	R3
0x10	RWWDCFG0	06h	R3
0x11	RWWDCFG1	09h	R3
0x12	WKTIMCFG0	00h	R2
0x13	WKTIMCFG1	00h	R2
0x14	WKTIMCFG2	00h	R2
0x15	DEVCTRL	00h	R2
0x16	DEVCTRLN	00h	R2
0x17	WWDSCMD	00h	R2
0x18	FWDRSP	00h	R2
0x19	FWDRSPSYNC	00h	R2
0x1A	SYSFAIL	00h	R1
0x1B	INITERR	00h	R2
0x1C	IF	00h	R2
0x1D	SYSSF	00h	R2
0x1E	WKSF	00h	R2
0x1F	SPISF	00h	R2
0x20	MONSF0	00h	R1
0x21	MONSF1	00h	R1
0x22	MONSF2	00h	R2
0x23	MONSF3	00h	R1
0x24	OTFAIL	00h	R1
0x25	OTWRNSF	00h	R2

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0x26	VMONSTAT	00h	R2
0x27	DEVSTAT	00h	R2
0x28	PROTSTAT	01h	R1
0x29	WWDSTAT	00h	R3
0x2A	FWDSTAT0	30h	R3
0x2B	FWDSTAT1	00h	R3
0x2C	ABIST_CTRL0	00h	[7:4]: R1 [3:0]: R2
0x2D	ABIST_CTRL1	00h	R2
0x2E	ABIST_SELECT0	00h	R2
0x2F	ABIST_SELECT1	00h	R2
0x30	ABIST_SELECT2	00h	R2
0x31	BCK_FREQ_CHANGE	00h	R2
0x32	BCK_FRE_SPREAD	00h	R2
0x33	BCK_MAIN_CTRL	00h	R2
0x3A	FWD_KEY	00h	R2
0x3B	MONSF4	00h	R2
0x3C	MCSMON	00h	R2
0x3D	CHIPCODE	-	R0
0x3F	GTM	02h	R2

13.3 Detailed Description

DEVCFG0 [7:0]				
ADDRESS: 0x00				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	WKTIMEN	RW	Wake timer enable	0 = Wake timer disabled 1 = Wake timer enabled in SLEEP or STANDBY state
[6]	WKTIMCYC	RW	Wake timer cycle period	when select short config: 0 = 8us 1 = 8.192ms when select long config: 0 = 1ms 1 = 1s

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[5]	WKTIMCYC_SEL	RW	Wake timer cycle period pre-scaler Wake timer cycle period selection for long timer	0 = Short config 1 = Long config
[4]	RSV	R	Reserved	
[3:0]	TRDEL	RW	Transition delay into low power states. For STANDBY and SLEEP transition. Defined as a step of 100 us.	0000 = 100us; 0001 = 200us; 0010 = 300us; 0011 = 400us; 0100 = 500us; 0101 = 600us; 0110 = 700us; 0111 = 800us; 1000 = 900us; 1001 = 1000us; 1010 = 1100us; 1011 = 1200us; 1100 = 1300us; 1101 = 1400us; 1110 = 1500us; 1111 = 1600us

DEVCFG1 [7:0]				
ADDRESS: 0x01				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	RSV	R	Reserved	
[3:0]	RESDEL	RW	Reset release delay time	0000 = 200us; 0001 = 400us; 0010 = 800us; 0011 = 1ms; 0100 = 2ms; 0101 = 4ms; 0110 = 10ms; 0111 = 15ms; 1000 = 30ms; 1001 = 60ms; 1010 = 100ms; others = 10ms.

DEVCFG2 [7:0]				
ADDRESS: 0x02				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	EVCEN	R	External core supply enable status	0 = External core supply disabled 1 = External core supply enabled
[6]	EN_BST	R	Step-up converter enable status	0 = Disabled 1 = Enabled
[5]	FRE	R	Step-down converter frequency selection status	0 = Step-down converter runs on low frequency range 1 = Step-down converter runs on high frequency range
[4]	CMONEN	RW	LDO_UC current monitor enable for transition to a low power state For STANDBY and SLEEP transition. The setting is overwritten in SLEEP as current monitoring is always enabled.	0 = Disabled 1 = Enabled

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ADDRESS: 0x03				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	CTHR	RW	Protection key Protection key register to request write access to protected registers. Unlock: write 32-bit sequence of 4 consecutive bytes (1: 0xAB 2:0xEF 3:0x56 4:0x12) to unlock access to protected registers. Lock: write 32-bit sequence of 4 consecutive bytes (1: 0xDF 2:0x34 3:0xBE 4:0xCA) to lock access to protected registers. All configured values are applied to SSC and WD module after the lock.	ABh = Key 1 to unlock protected registers. EFh = Key 2 to unlock protected registers. 56h = Key 3 to unlock protected registers. 12h = Key 4 to unlock protected registers. DFh = Key 1 to lock protected registers. 34h = Key 2 to lock protected registers. BEh = Key 3 to lock protected registers. CAh = Key 4 to lock protected registers.

SYSPCFG0 [7:0]				
ADDRESS: 0x04				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:1]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[0]	STBYEN	RW	Request standby regulator VO_STB enable	0 = Disabled 1 = Enabled

SYSPCFG1 [7:0]				
ADDRESS: 0x05				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	SS2DEL	RWP	Request safe state 2 delay Applied for transitions from NORMAL to INIT, WAKE and SLEEP state.	000 = no delay; 001 = 10ms; 010 = 50ms; 011 = 100ms; 100 = 250ms; 101 = 1250ms; 110 = 2500ms
[4]	ERRSLPEN	RWP	Request ERR pin monitor functionality enable while the system is in SLEEP	0 = ERRIN pin monitor is disabled in SLEEP 1 = ERRIN pin monitor can be active in SLEEP depending on ERREN bit value.
[3]	ERREN	RWP	Request ERRIN pin monitor enable	0 = Step-down converter runs on low frequency range 1 = Step-down converter runs on high frequency range
[2]	ERRRECEN	RWP	Request ERRIN pin monitor recovery enable	0 = Disabled 1 = Enabled
[1:0]	ERRREC	RWP	Request ERRIN pin monitor recovery time	00 = 1ms; 01 = 2.5ms; 10 = 5ms; 11 = 10ms

WDCFG0 [7:0]				
ADDRESS: 0x06				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	WWDETHR	RWP	Request window watchdog error threshold	WWD error thrshold = WWDETHR[3:0] * 1 times

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			Current configuration of ERR pin monitor recovery enable.	
[1:0]	ERRREC	R	Request watchdog cycle time	00 = 1ms; 01 = 2.5ms; 10 = 5ms; 11 = 10ms

RWDCFG0 [7:0]				
ADDRESS: 0x0D				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	WWDETHR	R	Window watchdog error threshold status Current configuration of WWD error threshold to generate reset and enter into INIT state	WWD error thrshold = WWDETHR[3:0] * 1 times
[3]	WWDEN	R	Window watchdog enable status Current configuration of WWD enable.	0 = Disabled 1 = Enabled
[2]	FWDEN	R	ERRIN pin monitor enable status Current configuration of ERR pin monitor enable.	0 = Disabled 1 = Enabled
[1]	WWDTSEL	R	Window watchdog trigger selection status Current configuration of WWD trigger selection. This is ignored when window watchdog is disabled.	0 = External WDI input used as a WWD trigger 1 = WWD is triggered by SPI write to WWDSCMD register
[0]	WDCYC	R	Request watchdog cycle time	0 = 0.1 ms tick period 1 = 1 ms tick period

RWDCFG1 [7:0]				
ADDRESS: 0x0E				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[6]	WDCYCDIV	R	Request enable of additional divider by 10 for watchdog cycle time (WDCYC) configuration, Data bits are sent inverted to SPI upon read access.	0 = Disabled 1 = Enabled, additional divider by 10 for watchdog cycle time (WDCYC) configuration is enabled
[5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4]	WDSLPEN	R	Request watchdog functionality enable while the device is in SLEEP	0 = Disabled 1 = Enabled, the WD will work based on individual configuration (WWDEN & FWDEN) settings while the system is in SLEEP mode
[3:0]	FWDETHR	R	Request functional watchdog error threshold FWD error threshold to generate reset and enter into INIT state.	FWD error thrshold = FWDETHR[3:0] * 1 times

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				0 = LDO_COM will be enabled after valid request
[4]	RSV	R	Reserved	
[3]	VREFEN	RW	Request voltage reference LDO_VRF enable	1 = LDO_VRF will be disabled after valid request 0 = LDO_VRF will be enabled after valid request
[2:0]	STATEREQ	RWHC	Request for device state transition Cleared to 000 by the HW after the request is processed. After writing a new state value a user should not change the value before it's cleared by HW.	000 = RESERVED; 001 = RESERVED; 010 = WAKE; 011 = STANDBY; 100 = SLEEP; 101 = NORMAL; 110 = INIT; 111 = NONE

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IF [7:0]				
ADDRESS: 0x1C				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	INTMISS	R	Interrupt not serviced in time flag Interrupt has not been serviced within tINT,TO time	0 = No interrupt timeout happened 1 = Interrupt timeout happened, cleared by hardware when all other flags in IF are cleared.
[6]	ABIST	RW1C	Requested ABIST operation performed flag	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag
[5]	OTF	RW1C	Over temperature failure interrupt flag	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag, read OTFAIL for details
[4]	OTW	RW1C	Over temperature warning interrupt flag	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag, read OTWRNSF for details
[3]	MON	RW1C	Monitor interrupt flag	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag, read MONSF0, MONSF1, MONSF2 and MONSF3 for details
[2]	SPI	RW1C	SPI interrupt flag	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag, read SPISF for details
[1]	WK	RW1C	Wake interrupt flag Only set if device generates an interrupt when leaving SLEEP state.	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag, read WKSF for details
[0]	SYS	RW1C	System interrupt flag	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag, read SYSSF for details

SYSSF [7:0]				
ADDRESS: 0x1D				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RSV	R	Reserved	
[5]	NO_OP	RW1C	State transition request failure flag Requested state transition via DEVCTRL & DEVCTRLN could not be performed because of wrong protocol.	0 = Write 0 - no action 1 = Event detected, write 1 to clear277 0 Td (5-1.1

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[2]	ADDRE	RW1C	SPI address invalid flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	LENE	RW1C	SPI frame length invalid flag Number of detected SPI clock cycles different than 16.	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	PARE	RW1C	SPI frame parity error flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

MONSF0 [7:0]				
ADDRESS: 0x20				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2SG	RW1C	Tracker2 short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[6]	TRK1SG	RW1C	Tracker1 short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[5]	VREFSG	RW1C	Voltage reference short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[4]	COMSG	RW1C	Communication LDO short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	VEXTSG	RW1C	External voltage short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	STBYSG	RW1C	Standby LDO short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	UCSG	RW1C	uC LDO short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	BK1SG	RW1C	Pre-Buck1 voltage short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

MONSF1 [7:0]				
ADDRESS: 0x21				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2OV	RW1C	Tracker2 over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[6]	TRK1OV	RW1C	Tracker1 over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[5]	VREFOV	RW1C	Voltage reference over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

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[4]	COMOV	RW1C	Communication LDO over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	VEXTOV	RW1C	External voltage over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	STBYOV	RW1C	Standby LDO over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	UCOV	RW1C	uC LDO over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	BK1OV	RW1C	Pre-Buck1 voltage over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

MONSF2 [7:0]				
ADDRESS: 0x22				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2UV	RW1C	Tracker2 under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[6]	TRK1UV	RW1C	Tracker1 under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[5]	VREFUV	RW1C	Voltage reference under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[4]	COMUV	RW1C	Communication LDO under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	VEXTUV	RW1C	External voltage under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	STBYUV	RW1C	Standby LDO under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	UCUV	RW1C	uC LDO under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	BK1UV	RW1C	Pre-Buck1 voltage under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

MONSF3 [7:0]				
ADDRESS: 0x23				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	BIASHI	RW1C	Bias current too high flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[6]	BIASLOW	RW1C	Bias current too low flag	0 = Write 0 - no action

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			1 = Event detected, write 1 to clear the flag
BG12OV	RW1C	Bandgap comparator over voltage condition flag (VBG1 ≥ VBG2 + 4%)	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
BG12UV	RW1C	Bandgap comparator under voltage condition flag (VBG1 ≤ VBG2 - 4%)	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
RSV	R	Reserved	
VBATOV	RW1C	Supply voltage VSUP over voltage flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

L [7:0]

ESS: 0x24

FIELD	TYPE	DESCRIPTION	DECODE
MON	RW1C	Monitoring over temperature flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
RSV	R	Reserved	
COM	RW1C	Communication LDO over temperature flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
RSV	R	Reserved	
UC	RW1C	uC LDO over temperature f 0.96 0Q q 2005-12.2 ( )0.6 (t1.4 re) 87.6 417D 60 >>BDC 0	

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				1 = Event detected, write 1 to clear the flag

VMONSTAT

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[7]	KEY4OK	R	Key4 ok status Information about validity of the 4th received protection key byte	0 = Key not valid 1 = Key valid
[6]	KEY3OK	R	Key3 ok status Information about validity of the 3rd received protection key byte	0 = Key not valid 1 = Key valid
[5]	KEY2OK	R	Key2 ok status Information about validity of the 2nd received protection key byte	0 = Key not valid 1 = Key valid
[4]	KEY1OK	R	Key1 ok status Information about validity of the 1st received protection key byte	0 = Key not valid 1 = Key valid
[3:1]	RSV	R	Reserved	
[0]	LOCK	R	Protected register lock status	0 = Access is unlocked 1 = Access is locked

WWDSTAT [7:0]				
ADDRESS: 0x29				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	RSV	R	Reserved	
[3:0]	WWDECNT	R	Window watchdog error counter status	WWD error counter = WWDECNT[3:0]*1 times

FWDSTAT0 [7:0]				
ADDRESS: 0x2A				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	RSV	R	Reserved	
[6]	FWDRSPOK	R	Functional watchdog response check error status	0 = Response message is wrong 1 = All received bytes in response message are correct
[5:4]	FWDRSPC	R	Functional watchdog response counter value	
[3:0]	FWDQUEST	R	Functional watchdog question	

FWDSTAT1 [7:0]				
ADDRESS: 0x2B				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	RSV	R	Reserved	
[3:0]	FWDECNT	R	Functional watchdog error counter value	FWD error counter = FWDECNT[3:0]*1 times

ABIST_CTRL0 [7:0]				
ADDRESS: 0x2C				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	STATUS	R	ABIST global error status ABIST status information after requested operation has been performed, information shall only be	5 = Selected ABIST operation performed with no errors 10 = Selected ABIST operation performed with errors, check respective

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				comparator, bit will be set in case of ABIST fail for this comparator
[2]	STBYUV	RWHU	Select Standby LDO UV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[1]	UCUV	RWHU	Select uC LDO UV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[0]	PREGUV	RWHU	Select Pre-regulator UV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

ABIST_SELECT2 [7:0]				
ADDRESS: 0x30				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	BIASHI	RWHU	Bias current too high flag	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[6]	BIASLOW	RWHU	Bias current too low flag	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[5]	BG12OV	RWHU	Bandgap comparator over voltage condition flag (VBG1 ≥ VBG2 + 4%)	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[4]	BG12UV	RWHU	Bandgap comparator under voltage condition flag (VBG1 ≤ VBG2 - 4%)	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[3]	INTOV	RWHU	Select internal supply OV condition	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[2:1]	RSV	R	Reserved	
[0]	VBATOV	RWHU	Supply voltage VSUP over voltage flag	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

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BCK_FREQ_CHANGE [7:0]
ADDRESS: 0x31
0*

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			configuration write 1 to update and write 0 after BUSY flag is cleared to proceed operation)	
[5:1]	RSV	R	Reserved	
[0]	RSV	R	Reserved	

FWD_KEY [7:0]				
ADDRESS: 0x3A				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	FWD_KEY	R	Function watchdog's respone	

SYS_STAT1 [7:0]				
ADDRESS: 0x3B				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RSV	R	Reserved	N/A
[5]	BOOST_OC	RW1C	Boost over current status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[4]	GNDLOSS	RW1C	GND loss status flag	
[3]	UC_OPEN	RW1C	UC LDO cap open status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	COM_OPEN	RW1C	Com LDO cap open status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	VREF_OPEN	RW1C	Vref LDO cap open status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	RSV	R	Reserved	N/A

SYS_STAT2 [7:0]				
ADDRESS: 0x3C				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	PROG	RW	MCU programming support enable(OR combination with PROG pin)	0 = Disabled via SPI(unless enabled by PROG pin high) 1 = Enabled via SPI(independent of PROG pin)
[6]	MPSIN	R	MCU programming support enable(OR combination with PROG bitfield)	0 = Disabled via pin PROG(unless enabled by PROG bitfield being set) 1 = Enabled via pin PROG(independent of PROG bitfield)
[5:0]	CYCMON	R	Watchdog cycle timer monitor	0D 0 wd cycles passed 1D 1 wd cycles passed 2D 2 wd cycles passed ... 50D 50 wd cycles passed 51D not used

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				... 63D not used

CHIP_CODE [7:0]				
ADDRESS: 0x3D				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	CHIP_CODE	RW	Chip Suffix Code	Chip Suffix Code, refer to Rev Note.

GTM [7:0]				
ADDRESS: 0x3F				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:2]	RSV	R	Reserved	N/A
[1]	NTM	R	Test mode inveted status	0 = Device is in test mode 1 = Device is in normal mode
[0]	TM	R	Test mode status	0 = Device is in normal mode 1 = Device is in test mode

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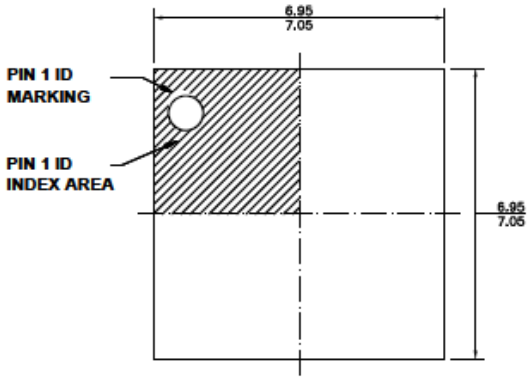
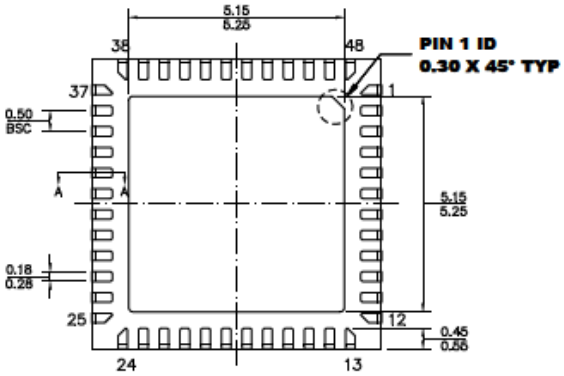
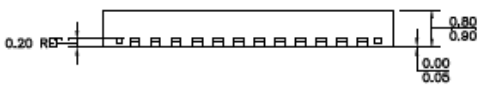
CCCCCCCCCCCCCC CCCCCC



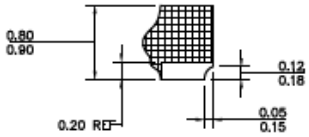
TOP VIEW



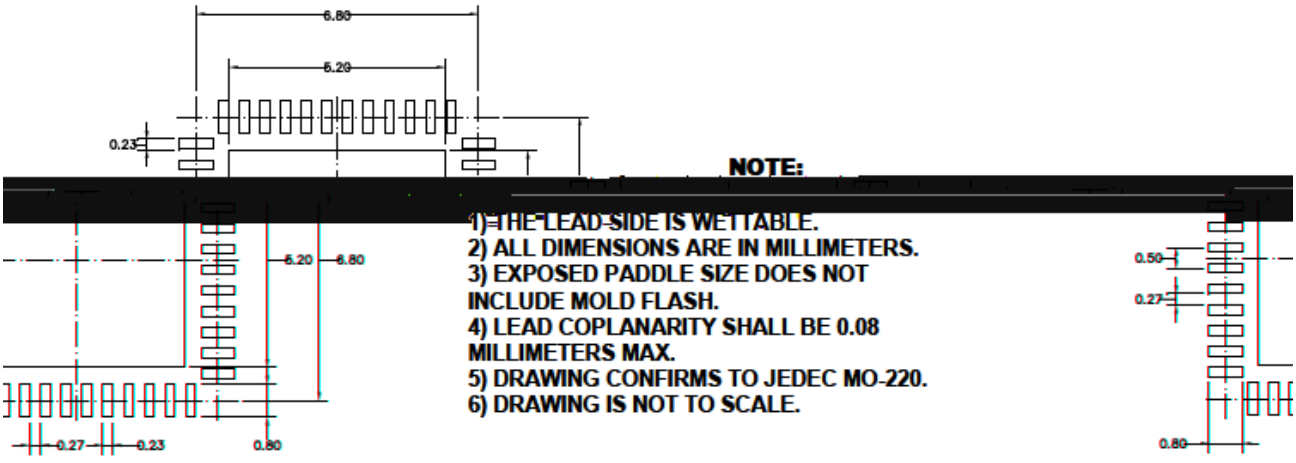
BOTTOM VIEW



SIDE VIEW



SECTION A-A



NOTE:

1) THE LEAD-SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) DRAWING CONFIRMS TO JEDEC MO-220.
6) DRAWING IS NOT TO SCALE.

ENDED LAND PATTERN

RECOMM

C

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