ASIL-D Safety Power Management IC for Safety Applications

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Wide Input Voltage Range:
  - 3.0V-40V with pre-boost regulator
  - 6.0V-40V without pre-boost regulator
- Asynchronous Pre-Boost Controller VO_BST:
  - Fixed Output Voltage of 7.5V
  - Maximum Duty Cycle up to 95%
  - Fixed 500kHz Switching Frequency
- Synchronous Pre-Buck1 Converter VO_BUCK1:
  - Fixed Output Voltage of 5.8V/5V/4V/3.3V
  - Up to 4A Continuous Output Current
  - Integrated 120 -Side and 90 Low-Side Power MOSFETs
  - Selectable 400kHz or 2.2MHz Switching Frequency
- Synchronous Post-Buck2 Converter VO_BUCK2:
  - Output Voltage Range from 0.6V to 1.87V
  - +/- 1.5% Output Voltage Accuracy
  - Up to 5A Continuous Output Current
  - Integrated 160 -Side and 100 Low-Side Power MOSFETs
  - Fixed 2.2MHz Switching Frequency
- LDO1 VO_UC for C Supply:
  - Selectable 5V/3.3V/1.8V Output Voltage
  - +/- 2% Output Voltage Accuracy
  - Up to 800mA Continuous Output Current
- LDO2 VO_COM for Communication Supply:
  - Selectable 5V/3.3V/1.8V Output Voltage
  - +/- 2% Output Voltage Accuracy
  - Up to 600mA Continuous Output Current
- Dual Tracker LDO3,4 VO_TRK1, VO_TRK2:
  - +/- 1% Accuracy under 5V Output Voltage or +/- 10mV Accuracy under tracking mode
  - Selectable 5V/3.3V/1.8V or VREF tracking mode Output Voltage
  - Up to 200mA Continuous Output Current
- LDO5 VO_VREF for Voltage Reference:
  - Selectable 5V/3.3V/1.8V Output Voltage
  - +/- 1% Output Voltage Accuracy
  - Up to 200mA Continuous Output Current
- LDO6 VO_STB for Standby Supply:
  - Selectable 3.3V or 5V Output Voltage
  - +/- 4% Output Voltage Accuracy
  - Up to 20mA Continuous Output Current
- Integrated Frequency Dither for EMI Mitigation
- Safe State Outputs SS1, SS2
- Reset Output

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PIN FUNCTIONS

NAME	NO.	DESCRIPTION
PGND_BST	1	Boost driver ground. Connect this pin to ground at the low side of Boost external current sense resistor to decouple the driver noise from the sensitive ground. If Boost is not used, connect this pin to ground directly.
VIN_STB	2	Standby LDO voltage input. Connect this input to supply (battery) voltage with reverse protection diode and capacitor between pin and ground. An EMC filter is recommended.
EN	3	Enable Input. A positive edge signal at this pin will wake the device. Connect to ground if not used.
WAKE	4	Wake Input. A high level signal of defined length at this pin will wake the device. In case of not used, connect to ground.
VO_STB	5	Output standby LDO. Connect a capacitor as close as possible to pin.
AGND1	6	Analogue ground, pin 1. Connect this pin directly (low ohmic and low inductive) to ground.
AGND2	7	Analogue ground, pin 2. Connect this pin directly (low ohmic and low inductive) to ground.
AGND_S1	8	Analogue ground, safety, pin 1. Connect this pin directly (low ohmic and low inductive) to ground. In case a safety switch is used, connect directly to the source of the NMOS used.
AGND_S2	9	Analogue ground, safety, pin 2. Connect this pin directly (low ohmic and low inductive) to ground. In case a safety switch is used, connect directly to the source of the NMOS used.
SS2	10	Safe state output signal 2, sets the application into a safe state. Signal is delayed against SS1, delay can be adjusted via SPI command.
SS1	11	Safe state output signal 1, sets the application into a safe state.
SDI	12	Serial peripheral interface, signal data input. SPI signalling port, connect to SPI port “data output” of micro processor to receive commands during SPI communication.
SDO	13	Serial peripheral interface, signal data output. SPI signalling port, connect to SPI port “data input” of micro processor to send status information during SPI communication. If not used, leave open.
SCL	14	Serial peripheral signal clock. SPI signalling port, connect to SPI port “clock” of micro processor to clock the device for SPI communication.
CSB	15	Serial peripheral interface, signal chip select. SPI signalling port, connect to SPI port “chip select” of micro processor to address the device for SPI communication. If not used, leave open.
WDI	16	Watchdog input, trigger signal. Input for trigger signal, connect the “trigger signal output” of the micro processor to this pin. In case of not used, leave open (internal pull-down).
RESETB	17	Reset output. Open drain structure with internal pull-up current source. A low signal at this pin indicates a reset event.
INTB	18	Interrupt signal. Push-pull-stage. A low pulse at this pin indicates an interrupt, the micro processor shall read out the SPI status registers. Connect to a non maskable interrupt port (NMI) of the micro processor core supply voltage.
SYNCO	19	Synchronization output signal. Connect this output to the optional external switch mode post regulator synchronization input. The signal delivers the buck regulator switching frequency either in phase or shifted by 180° (selectable via SPI command). The switch mode post regulator shall synchronize to the rising edge. If not used, leave open.

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PIN FUNCTIONS (continued)

NAME	NO.	DESCRIPTION
ERRIN	20	Error signal input. Input for error signal from micro processor safety managing unit (SMU, internal failure detection of the micro processor). Connect the “error signal output” of the micro processor to this pin.
SEQ	21	Sequencer output to enable external post regulator for core supply. Connect this pin to the enable input of the external post regulator. If not used, leave open.
PROG	22	Microcontroller programming support pin. Pull down this pin to ground for operation. Optionally, this pin can be used for microcontroller debugging and programming purposes.
EN_EXT	23	Configuration pin for external post regulator for core supply. Connect this pin to ground if the option external post regulator is not used. If the option external post regulator is used, leave open.
FSW	24	Frequency adjustment pin. Connect pin to ground for low frequency range or leave open for high frequency range.
EN_BST	25	Configuration pin for boost converter. Connect this pin to ground if the option boost pre regulator is not used. If the option boost pre regulator is used, leave open.
VEXT	26	Input for optional external post regulator output voltage (core supply). Connect an external resistor divider to adjust the over and under voltage thresholds of reset output signal RESETB. If the option external post regulator is not used, leave open.
NC	27	Internally not connected: This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
AGND3	28	Analogue ground, pin 3. Connect this pin directly (low ohmic and low inductive) to ground.
VO_VREF	29	Output voltage reference. Connect a capacitor as close as possible to pin.
VO_UC	30	Output LDO_uC supply (micro processor supply). Connect a capacitor as close as possible to pin.
VO_COM	31	Output LDO_communication supply. Connect a capacitor as close as possible to pin.
VO_TRK2	32	Output tracker 2. Connect a capacitor as close as possible to pin.
VO_TRK1	33	Output tracker 1. Connect a capacitor as close as possible to pin.
PGND_BK2	34	Post-Buck2 power ground. Connect this pin straight (low ohmic and low inductive) to ground and post· regulator output capacitor minus.
SW_BK2	35	Switching node of Post-Buck2. Connect a power inductor to this pin.
VIN_BK2	36	Pre-Buck1 redundant feedback input plus input for LV step down post regulator: Connect the capacitor of the step down pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin VO_BK1.
VO_BK1	37	Pre-Buck1 feedback input. Connect the capacitor of the buck pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin VIN_LDO.
VIN_LDO	38	Input for linear post regulators and trackers. Connect the capacitor of the buck pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin VO_BK1.
VO_BK2	39	Post-Buck2 feedback input. Connect the capacitor of the LV step down post regulator output filter with low ohmic and low inductive connection straight to this pin.

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{BAT}	Operating Voltage Range with active Pre-Boost	3.0	40	V
T_J	Operating Junction Temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC-Q100-002	-2	2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-48	UNIT
R	Junction to ambient thermal resistance(1)	25.06	°C/W
JT	Junction-to-top characterization parameter	3.49	
JB	Junction-to-board characterization parameter(1)	9.1	
R (top)	Junction to case (top) thermal resistance(1)	19.5	
R B	Junction to board thermal resistance(1)	9.53	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT61490S is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT61490S. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

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ELECTRICAL CHARACTERISTICS

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{SUP}	Operating input voltage at VSUP pin		6		40	V
V_{SUP_UVLO}	Input UVLO	V_{SUP} rising	4.35	4.6	4.85	V
$V_{SUP\_UVLO\_HYS}$	Hysteresis			1.6		V
V_{SUP_OVP}	Input OVP	V_{SUP} rising	42	44	46	V
$V_{SUP\_OVP\_HYS}$	Hysteresis		1	2	3	V
$V_{START,STG,BUCK\_RISING}$	Step down regulator short to ground activation rising threshold at pin VSUP	V_{SUP} increasing	5.5	5.7	5.9	V
$V_{START,STG,BUCK\_HYS}$	Step down regulator short to ground activation threshold Hysteresis at pin VSUP			150		mV
I_Q(1)	Quiescent current from VSUP	In INIT/NORMAL/WAKE state, Boost is off, f_{OSC_BUCK1}=2.2MHz, FCCM(2)		16		mA
		In INIT/NORMAL/WAKE state, Boost is off, f_{OSC_BUCK1}=400kHz, FCCM(2)		8		mA
		In INIT/NORMAL/WAKE state, Boost is off, PFM(2)		3		mA
		In STANDBY state, Standby LDO is off, TJ=25°C		55	65	A
		In STANDBY state, Standby LDO is off, TJ=-40~150°C			150	A
		In STANDBY state, Standby LDO is on		70	100	A
		In SLEEP state		150	350	A
		In FAILSAFE state			1200	A
Enable Signal Input EN						
V_{EN_H}	Enable high threshold	V_{EN} ramping up		1.6	2	V
V_{EN_L}	Enable low threshold	V_{EN} ramping down	0.8	1.2		V
V_{EN_HYS}	Enable hysteresis			400		mV
$T_{EN\_DEGLITCH}$	Enable high deglitch time		20			s
I_{EN_HIGH}	Enable high input current	V_{EN} = 16V		8	15	A
I_{EN_LOW}	Enable low input current	V_{EN} = 0.5V		0.1	2	A
Wake Signal Input WAKE						
V_{WAKE_H}	Wake high threshold	V_{WAKE} ramping up		1.6	2	V
V_{WAKE_L}	Wake low threshold	V_{WAKE} ramping down	0.8	1.2		V
V_{WAKE_HYS}	Wake hysteresis			400		mV
$T_{WAKE\_DEGLITCH}$	Wake high deglitch time		40			s

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{SYN_LO}	SYNC output low level	V_{VUC} = 3.3V, I_{SYNC} = 5.5mA			0.7	V
D_{SYNC}	SYNC output duty cycle			50		%
RESETB Timing						
t_{CYCLE}	Reset cycle time		9.4	10	10.65	
t_{RD}	Reset delay time,	Default option		1000		t_{CYCLE}
		Adjustable Range	20		1500	t_{CYCLE}
t_{RR}	Reset reaction time		8		20	
t_{RR_STB}	Reset reaction time of standby LDO		8		40	
t_{STG}	Short to ground detection time	LDO	2.7	3	3.3	ms
		Pre-Buck1, 2.2MHz switching frequency	2.7	3	3.3	ms
		Pre-Buck1, 400kHz switching frequency	5.4	6	6.6	ms
t_{SHUT}	System shutdown time		9		20	ms
RESETB OV/UV Threshold for Standby LDO VSTB						
$V_{OV\_THR\_VSTB}$	Over voltage reset threshold	5V output	105	107	109	%
		3.3V output	105	107	109	%
$V_{OV\_HYS\_VSTB}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
$V_{UV\_THR\_VSTB}$	Under voltage reset threshold	5V output, option 0	84	86	88	%
		5V output, option 1	88	90	92	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	90	92	94	%
$V_{UV\_HYS\_VSTB}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
RESETB OV/UV Threshold for LDO VUC						
$V_{OV\_THR\_VUC}$	Over voltage reset threshold	5V output	105	107	109	%
		3.3V output	105	107	109	%
$V_{OV\_HYS\_VUC}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
$V_{UV\_THR\_VUC}$	Under voltage reset threshold	5V output, option 0	84	86	88	%
		5V output, option 1	88	90	92	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	90	92	94	%
$V_{UV\_HYS\_VUC}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
RESETB OV/UV Threshold for LDO VCOM						
$V_{OV\_THR\_VCOM}$	Over voltage reset threshold	5V output, option 0	108	110	112	%
		5V output, option 1	103	105	107	%
		3.3V output, option 0	105	107	109	%
		3.3V output, option 1	103	105	107	%
$V_{OV\_HYS\_VCOM}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
$V_{UV\_THR\_VCOM}$	Under voltage reset threshold	5V output, option 0	88	90	92	%
		5V output, option 1	93	95	97	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	90	92	94	%
$V_{UV\_HYS\_VCOM}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
RESETB OV/UV Threshold for LDO VREF						
$V_{OV\_THR\_VREF}$	Over voltage reset threshold	5V output, option 0	105	107	109	%
		5V output, option 1	102	104	106	%
		3.3V output, option 0	105	107	109	%
		3.3V output, option 1	104	106	108	%
$V_{OV\_HYS\_VREF}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
$V_{UV\_THR\_VREF}$	Under voltage reset threshold	5V output, option 0	84	86	88	%

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{UV\_THR\_VTRK1}$	Under voltage reset threshold	5V output, option 0	88	90	92	%
		5V output, option 1	90	92	94	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	90	92	94	%
$V_{UV\_HYS\_VTRK1}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
RESETB OV/UV Threshold for Tracker VTRK2						
$V_{OV\_THR\_VTRK2}$	Over voltage reset threshold	5V output, option 0	108	110	112	%
		5V output, option 1	106	108	110	%
		3.3V output	105	107	109	%
$V_{OV\_HYS\_VTRK2}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
$V_{UV\_THR\_VTRK2}$	Under voltage reset threshold	5V output, option 0	88	90	92	%
		5V output, option 1	90	92	94	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	90	92	94	%
$V_{UV\_HYS\_VTRK2}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
RESETB OV/UV Threshold for Pre-Buck1						
$V_{OV\_THR\_VBK1}$	Over voltage reset threshold		111	113	115	%
$V_{OV\_HYS\_VBK1}$	Over voltage reset hysteresis		40	60	90	mV
$V_{UV\_THR\_VBK1}$	Under voltage reset threshold		86	88	90	%
$V_{UV\_HYS\_VBK1}$	Under voltage reset hysteresis		40	60	90	mV
RESETB OV/UV Threshold for VEXT						
$V_{OV\_THR\_VEXT}$	Over voltage reset threshold	Option0	107.5	109	110.5	%
		Option1	106.5	108	109.5	%
$V_{OV\_HYS\_VEXT}$	Over voltage reset hysteresis		5	8	15	mV
$V_{UV\_THR\_VEXT}$	Under voltage reset threshold	Option0	89.5	91	92.5	%
		Option1	90.5	92	91.5	%
$V_{UV\_HYS\_VEXT}$	Under voltage reset hysteresis		5	8	15	mV
I_{RSTB_PULL}	RESETB output, pull-up current	V_{RSTB} 2.0 V	-175	-110	-15	A

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
RESETB Output						
$_{RSTB\_L}$	RESETB output low level	V_{VUC} = 5V, I_{RSTB} = 7mA			0.7	V
		V_{VUC} = 5V, I_{RSTB} = 3.5mA			0.4	V
		V_{VUC} = 3.3V, I_{RSTB} = 5.5mA			0.7	V
		V_{VUC} = 3.3V, I_{RSTB} = 3mA			0.4	V
t_{RSTB_FALL}(2)	RESETB output fall time	C_{RSTB} = 50pF			25	ns
INTB Output						
V_{INTB_H}	Interrupt output high level	V_{VUC} = 5V, I_{INTB} = -9mA	4			V
		V_{VUC} = 3.3V, I_{INTB} = -7mA	2.3			V
V_{INTB_L}	Interrupt output low level	V_{VUC} = 5V, I_{INTB} = 7mA			0.7	V
		V_{VUC} = 3.3V, I_{INTB} = 5mA			0.7	V

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{ERR_L}	ERRIN valid low level				0.8	V
V_{ERR_HYS}	ERRIN hysteresis	V_{VUC} = 5V		350		mV
		V_{VUC} = 3.3V		160		mV
I_{ERR_PULL}	ERRIN pull-down current			150	330	A
C_{ERR}(2)	ERR input capacitance			4	15	pF
t_{ERR_VALID}	Valid ERRIN input signal frequency	Duty = 50%	10		45	kHz
$t_{ERR\_INVALID}$	Invalid ERRIN input signal frequency	Duty = 50%, low frequency	0		5	kHz
		Duty = 50%, high frequency	96.2		500	kHz
t_{ERR_DET}	Invalid ERRIN input signal detection time	Low frequency	50.1		99.9	s
		High frequency	5.2		11.1	s
t_{ERR_REAC}	ERRIN reactivation time-out	After SLEEP	9	10	11	ms
		After re-enabling via SPI	50.1		110	s
Safe State Indictor SSx						
V_{SSx_H}	SSx output high level	V_{VUC} = 5V, I_{SSx} 1mA	3.6	4.8	V_{VUC}	V
		V_{VUC} = 5V, I_{SSx} 5mA	3	4.3	V_{VUC}	V
		V_{VUC} = 3.3V, I_{SSx} 1mA	2.9	3.2	V_{VUC}	V
		V_{VUC} = 3.3V, I_{SSx} 5mA	2	2.8	V_{VUC}	V
R_{SSx}	SSx pull-down resistor		70	100	130	k
V_{SSx_L}	SSx output low level				0.8	V
t_{SSx}	SSx internal reaction time			12	30	s
t_{SSx_ACC}	SSx time base accuracy		-10		10	%
t_{REC}	Adjustable recovery delay time	Option0		0		ms
		Option1		1		ms
		Option2		2.5		ms
		Option3		5		ms
		Option4		10		ms
t_{SS_DLY}	Adjustable delay time between SS1 and SS2	Option0		0		ms
		Option1		10		ms
		Option2		50		ms
		Option3		100		ms
		Option4		250		ms
Watch Dog Interface						
t_{WD_PERIOD}	Watchdog period time	Option0	94	100	106	s
		Option1	940	1000	1060	s
t_{WD_OPEN}	Long open window time		564	600	639	ms

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{WD_SAMPLE}	Watchdog sampling time		188	200	213	s
V_{WDI_HI}	Threshold for WDI pin					

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{SEQ_DLY}	Sequential Transfer Delay		600			ns
		SLEEP state	2			s
t_{SPI_DUR}	Frame duration (CSB low)				1.85	ms

(1) All quiescent current are measured under T_J 85 C and 10V VIN 28V, no load, selectable options off (external regulators, watchdog, timers).
(2) Guaranteed by sample characterization, not tested in production.

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TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12V, V_{Buck1} = 5.8V, V_{Buck2} = 1.2V, V_{LDO1} ~ V_{LDO6}= 5V, L1 = 10uH, L2 = 1uH, T_A = 25°C, unless otherwise noted.

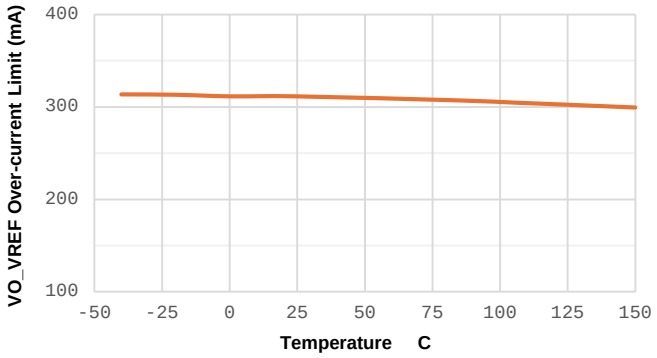

Figure 7. VO-VREF Over-current Limit vs. Temperature

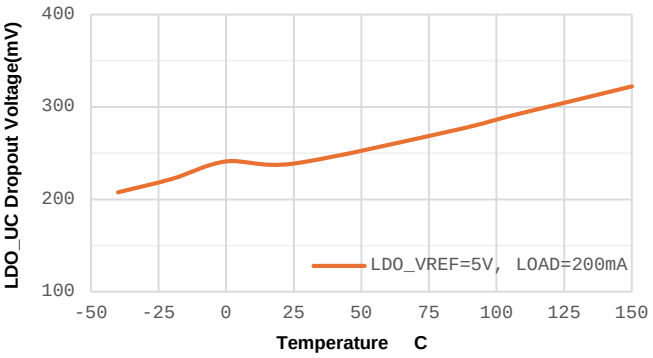

Figure 8. VO-VREF Dropout Voltage vs. Temperature

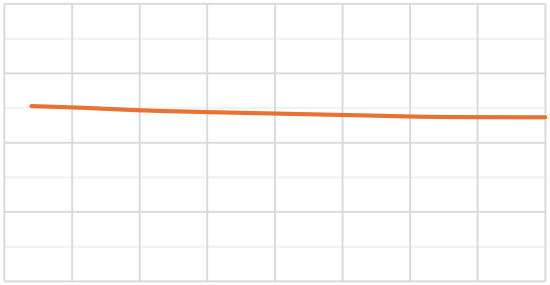

Figure 9. VO-STB Over-current Limit vs. Temperature

Figure 10. VO-STB Dropout Voltage vs. Temperature

Figure 11. VO-TRK1 Over-current Limit vs. Temperature

Figure 12. VO- TRK2 Dropout Voltage vs. Temperature

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FUNCTIONAL BLOCK DIAGRAM

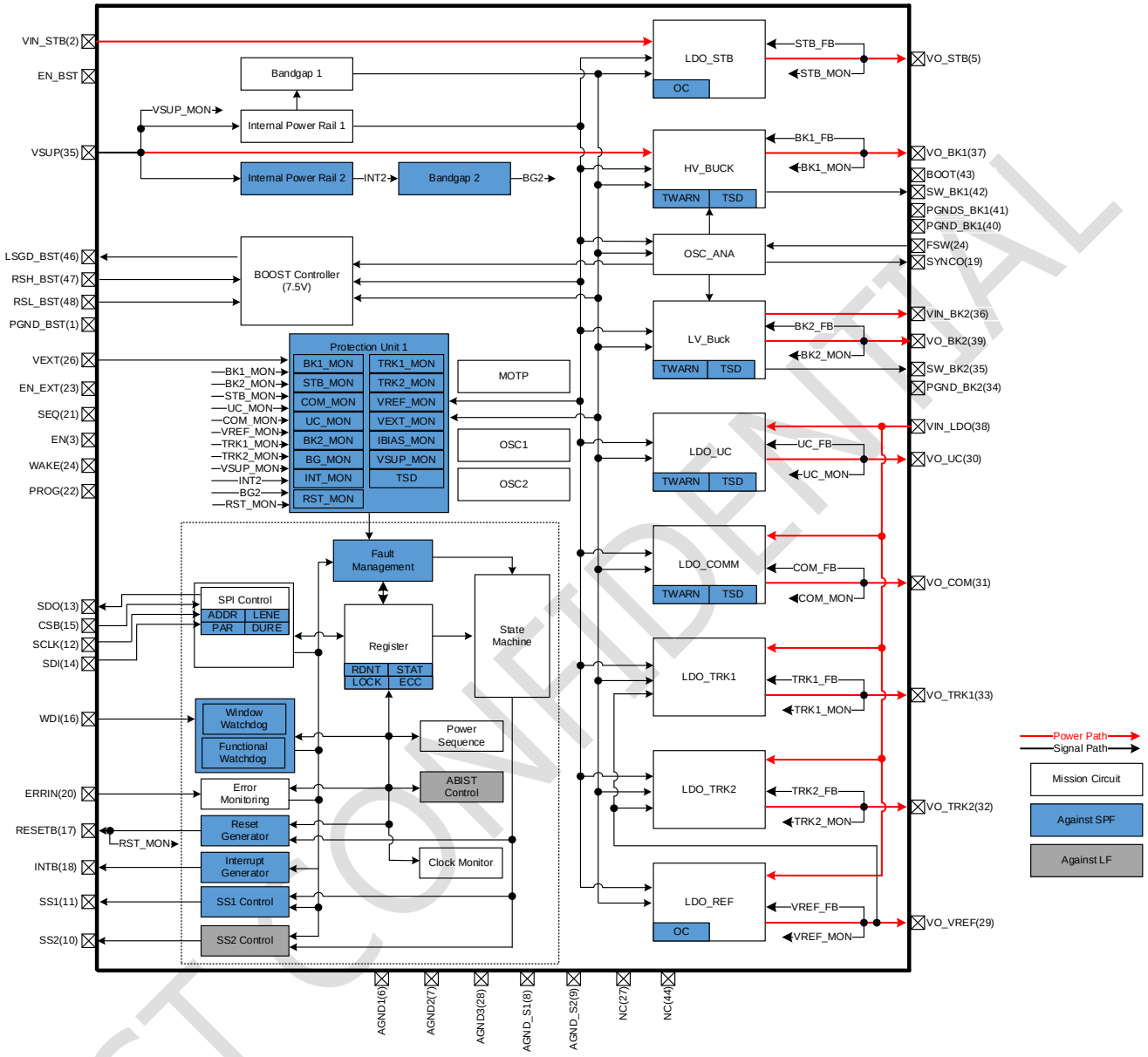

Figure 13. Functional Block Diagram

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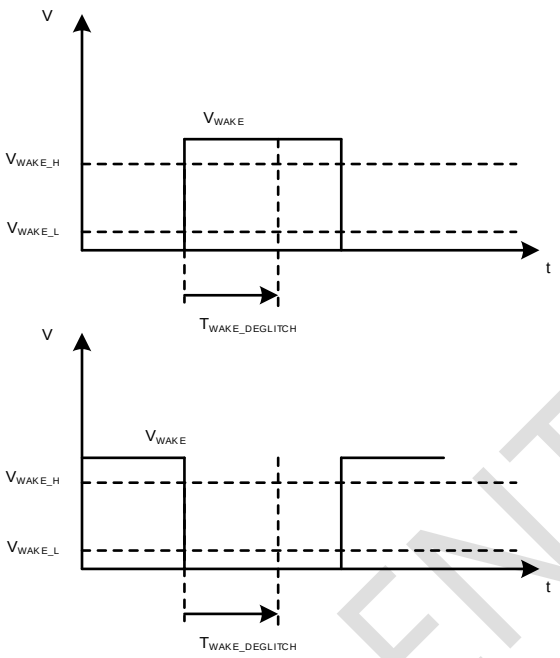


Figure 15. Valid wake signal

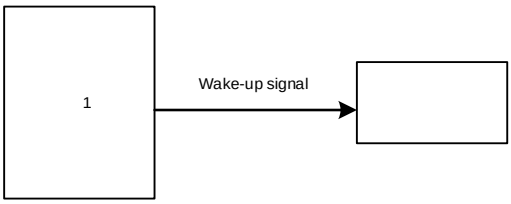
A valid Wake-up signal will bring the device from STANDBY to INIT state, from SLEEP to WAKE state or from FAILSAFE to INIT state.

A low signal V_{WAKE_L} at pin WAKE as well as a negative going edge at pin EN will have no impact on the state machine and will not initiate a transition between states.

In case a valid Wake-up signal is detected during the transition phase from NORMAL to SLEEP state, the device will initiate a transition to WAKE state and generate an interrupt.

In case a valid Wake-up signal is detected during the transition phase from NORMAL to STANDBY state, the device will initiate a transition to INIT state and a Reset (RESETB) will be generated.

Before sending a SPI transition command, pin EN doesn't have to be brought below V_{EN_L}. Even if pin EN is high (above V_{EN_H}), the SPI transition command will still send the device into SLEEP or STANDBY state.



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SPI.
For the chosen time-base is 1 s and a wake up time between 1 s to 194 days can be configured via SPI.
When entering STANDBY or SLEEP state, the counter is loaded with the value of the wake up timer register and starts decrementing. At underflow, the timer will wake up the device from either SLEEP or STANDBY state. When leaving SLEEP state, an interrupt will be generated. The remaining timer counter will be stored if the device wake up before the timer is expired, MCU can read back via SPI to calculate the corresponding time elapsed.

3 Pre Regulators

3.1 Introduction

The pre regulator is mandatory to maintain a stabilized and constant intermediate circuit voltage to supply the following post regulators. It consists of two independent regulators: A HV boost converter with an external power stage in front to maintain a minimum input voltage to the following HV buck converter.
The boost converter can be deactivated (if not needed) by connecting pin EN_BOOST to ground. Leaving pin EN_BOOST open activates the boost regulator.
The buck regulator frequency can be preset by leaving pin FSW open for the high switching frequency range or connecting to GND for the low switching frequency range.
The HV buck converter is constantly on, providing a stabilized intermediate circuit voltage VO_BK1 to supply the following post regulators. The boost converter is connected directly to the input voltage V_{Bat}. It only operates during low input voltage condition (i.e. cold crank) when the input voltage drops below the threshold $V_{PRE\_REG,boost,UV}$, to maintain an input voltage high enough for the following buck regulator. Low input voltage condition means, that the input voltage at pin VSUP is too low to provide an intermediate circuit voltage VO_BK1 within the specified limits. An internal comparator connected to the input voltage path detects the threshold when to turn on the boost converter. In case the input voltage is above the boost converter output voltage (threshold for switching on the boost converter), this regulator is deactivated by the internal comparator. An internal logic switches the boost converter on (and off again) whenever it is needed.

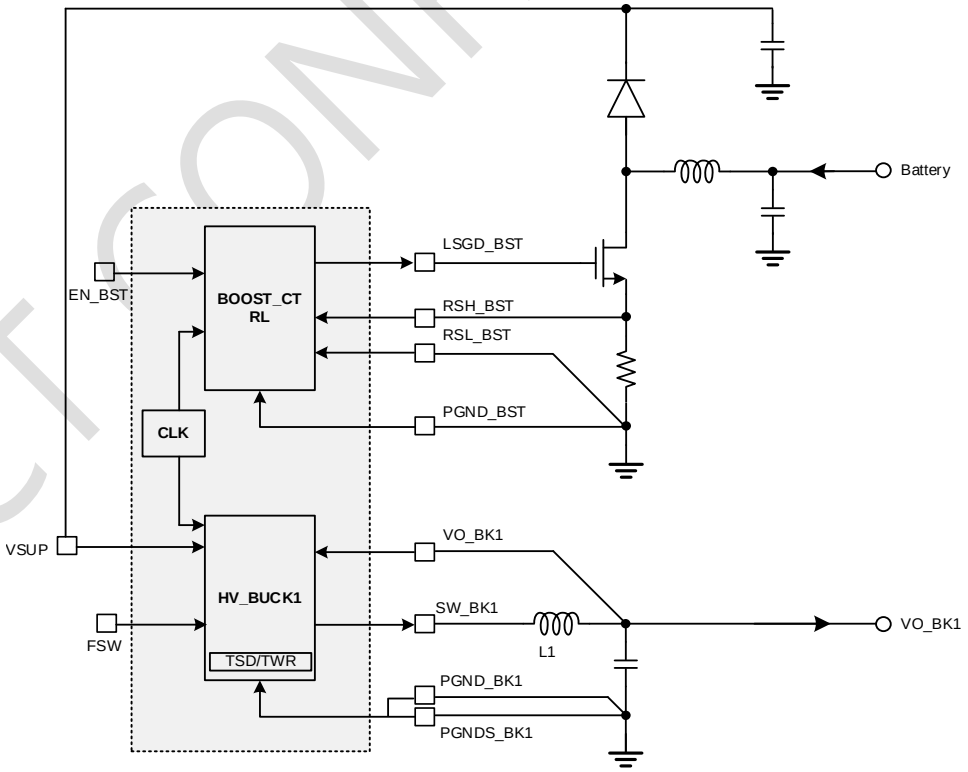

Figure 17. Principle of pre regulator stage

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regulator is supplied from the intermediate circuit voltage VO_BK1, which provides a stabilized voltage. The output voltage VO_VREF is controlled by the error amplifier. The actual value is compared to a reference voltage derived from band gap 1 for regulators. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR). The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.
Protection circuitry is installed to prevent the regulator and the application from damage:

• To protect the pass element of the LDO_VREF from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached the current will be limited, thus the output voltage will decrease. The regulator is protected against short circuit to ground.

• The output voltage is monitored by the voltage monitoring. In case of over voltage at pin VO_VREF, the LDO_VREF will be switched off and the device will move into FAILSAFE state. The event will be stored in an SPI status register (**MONSF1**). In case of under voltage at pin VO_VREF, the event will be indicated by an interrupt and stored in an SPI status register (**MONSF2**). The regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{STG}. If the under voltage should be present for more than t_{STG}, the regulator will be switched off. This event will be stored in an SPI status register (**MONSF0**) and an interrupt will be generated.

• There is no dedicated temperature sensor for this regulator. The temperature is sensed on the chip by other te exceed the pre warning threshold, an interrupt will indicate this event and it will be stored in a SPI status register (**OTWRNSF**). If the chip temperature will exceed the temperature shutdown threshold, the regulator will be switched off. The temperature switch off time will be at least one second. An overload at LDO LDO_VREF (over current detected for more than 1ms) will be indicated by an interrupt and it will be stored in a SPI status register (**OTWRNSF**).
If the device enters FAILSAFE state the RESETB is pulled low and all supplies are switched off.
The regulator LDO_VREF is switched off in STANDBY and FAILSAFE state. In INIT, SLEEP, NORMAL and WAKE state LDO_VREF is ON or OFF depending on the SPI configuration.
For further details please refer to **Chapter State Machine**.

4.5 Tracker 1 & 2

The linear trackers 1 and 2 offer a sensor supply with a very high accuracy referred to voltage reference output (pin VO_VREF).
Both trackers are supplied by the intermediate circuit voltage VO_BK1, which provides a stabilized voltage. The output voltage VO_TRKx is controlled by the error amplifier. The actual value is compared to a reference voltage provided by the reference voltage VO_VREF. The tracker output voltages follow the VO_VREF output with a very small drop. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor for each tracker should be chosen according the specified requirements (capacitance value and electrical series resistance ESR). The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.
Protection circuitry is installed to prevent damage to both trackers and the application:

• To protect the pass element of a tracker from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached, the current will be limited and in consequence the output voltage will decrease. A tracker is protected against short circuit to ground and short circuit to battery voltage.

• The output voltage is monitored by the voltage monitoring. In case of over voltage at pin VO_TRKx, the corresponding tracker will be switched off, the event will be stored in an SPI status register (MONSF1) and an interrupt will be generated. In case of under voltage at pin VO_TRKx, the event will be stored in an SPI status register (**MONSF2**) and an interrupt will be generated. The tracker will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{STG}. If the under voltage should be present for more than t_{STG}, the tracker will be switched off. This event will be stored in an SPI status register (**MONSF0**) and an interrupt will be generated.

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• The tracker is capable to withstand a short circuit either to ground or to battery voltage without receiving a damage. In case of a short circuit to battery voltage and if the battery voltage is above the tracker over voltage threshold, the tracker will be switched off, the event will be stored in the SPI status register (**MONSF1**).

• There is no dedicated temperature sensor for this regulator. The temperature is sensed on the chip by other exceed the pre warning threshold, the event will be stored in an SPI status register (**OTWRNSF**) and an interrupt will be generated. If the chip temperature exceeds the temperature shutdown threshold, the tracker will be switched off. The temperature switch off time is at least one second.

Both trackers are switched off in STANDBY and FAILSAFE. In INIT, NORMAL, SLEEP and WAKE state each tracker is ON or OFF depending on the SPI configuration.

4.6 Integrated LV Buck Regulator

The internal synchronous buck offers a 0.6-1.87V (with 10mV step) and up to 5A current capabilitys for core voltage supply. The LV buck2 is supplied by the intermediate circuit voltage VO_BK1.

The switching frequency of LV buck2 is fixed at 2.2MHz. The FSS circuitry shifts the switching frequency range and triangular or pseudo modulation. To further improve the EMI performance, the LV buck2 and HV buck1 will operate with 180° phase-shifted clock. The regulation loop operates in constant one time (COT) mode. Under normal load conditions the regulator operates in Forced continuous conduction mode (FCCM). Under light load conditions it will operate in Pulse Frequency Modulation (PFM) to minimize the internal current consumption (only in SLEEP state, not in NORMAL, WAKE or INIT state).

The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor for LV buck2 should be chosen at least 47uF and 100uF is recomended.

Protection circuitry is installed to prevent damage:

• To protect the pass element of a tracker from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached, the current will be limited and in consequence the output voltage will decrease.

• The output voltage is monitored by the voltage monitoring. In case of over voltage at pin VO_BK2, the LV buck2 will be switched off, and the device will move into FAILSAFE state. The event will be stored in the SPI status register (**MONSF1**). In case of under voltage at pin VO_BK2, the device will move into INIT state, pin RESETB will be pulled low and the event will be stored in an SPI status register (**MONSF2**). The regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{STG}. If the under voltage should be present for more than t_{STG}, the device will move into FAILSAFE state. This event will be stored in an SPI status register as well (**MONSF0**).

• The buck2 is capable to withstand a short circuit to ground. The event will be stored in the SPI status register (**MONSF1**).

• There is a dedicated temperature sensor for this regulator. The temperature is sensed on the power MOSFET of the buck2. In case of the chip temperature will exceed the pre warning threshold, the event will be stored in an SPI status register (**OTWRNSF**) and an interrupt will be generated. If the chip temperature exceeds the temperature shutdown threshold, the tracker will be switched off. The temperature switch off time is at least one second.

LV buck2 are switched off in STANDBY and FAILSAFE. In INIT, NORMAL, SLEEP and WAKE state LV buck2 is ON or OFF depending on the SPI configuration.

4.7 External Post Regulator for Core Supply (optional)

An additional external post regulator may be added to the SCT61490S to provide the core supply voltage for the

In this case the configuration pin EN_EXT has to be left open to indicate that the external core voltage supply option is active. The configuration of the EN_EXT pin will only be read during the power sequencing at the point the core supply would be started.

The regulator is fed from the intermediate circuit voltage VO_BK1. The post regulator is enabled by a high signal at

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pin SEQ and switched off by a low signal at pin SEQ. The SEQ signal is controlled by the state machine. For example a detection of over voltage at pin VEXT will create a low signal at pin SEQ and shut down the post regulator

The device offers a synchronization signal of 50% duty cycle at pin SYNCO equal in phase (only with a very small delay) and frequency or shifted by 180 degree to the internal step down pre regulator (the selection is done via SPI command). It is highly recommended to synchronize the external switch mode post regulator to this signal to avoid interferences. The external post regulator will be enabled as soon as the pre regulator output voltage VO_BK1 is present and the VO_UC is above the lower reset threshold.
The output voltage of the post regulator will be monitored by the reset function of the device. To obtain a proper monitoring the output voltage of the post regulator has to be connected to the voltage monitoring input at pin VEXT via a resistor divider. The resistor divider should be dimensioned to adjust the post regulator output voltage to the internal reset reference voltage.
The synchronization signal at pin SYNCO can be switched on via SPI command, default configuration is off. Protection circuitry should be installed to prevent the external regulator and the application from damage:

• To protect the pass device(s) of the external post regulator from overstress a current limitation function should limit the output current to the maximum specified limit. Current sensing should be done via a current mirror, no sense resistor should be used. In case the maximum current should occur, it will be limited, thus the output voltage will decrease. The regulator should be protected against short circuit to ground.

• The output voltage is monitored by the voltage monitoring of the SCT61490S, no further reset function is required on the external post regulator. In case such a reset function should be present, it will not be used or supported by the reset function of the SCT61490S. In case of over voltage at pin VEXT the external post regulator will be switched off by pulling pin SEQ to low and the SCT61490S will move into FAILSAFE state. The event will be stored in an SPI status register (**MONSF1**). In case of under voltage at pin VEXT, the device will move into INIT state, pin RESETB will be pulled low and the event will be stored in an SPI status register (**MONSF2**). The external post regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{StG}. If the under voltage is present for more than t_{STG}, the device will move into FAILSAFE state. This event will be stored in an SPI status register as well (**MONSF0**).

• There should be a temperature shutdown function at the external post regulator. If the power stage temperature should exceed the temperature shutdown threshold, the post regulator should be switched off by its own temperature shutdown. The SCT61490S will recognize this as an under voltage and react as described above.

4.8 Power Sequencing

The SCT61490S includes a power sequencing function to ensure a proper ramping up of all output voltages. After the internal Power-On-Reset (POR) is released the standby regulator and the pre regulator start to operate.
In case of one of the microcontroller related voltages (VO_STB, VO_UC, VO_BK1, VO_BK2 or VEXT) cannot be ramped up (e.g. short to GND), the power sequence is stopped and reset output is asserted. The device will move to FAILSAFE state.
In case of one of the non microcontroller related voltages (VO_VREF, VO_COM, VO_TRK1 or VO_TRK2) cannot be ramped up (e.g. short to GND), the power sequence is stopped, but the reset output is still released after the power on reset delay time t_{RD}. The microcontroller should check the status of the outputs by reading the SPI status register (**VMONSTAT**).
In case the microcontroller is sending a SPI request to enable or disable any non microcontroller related LDO (VO_VREF, VO_COM, VO_TRK1 or VO_TRK2) during the power sequencing, the sequence will be stopped and the requested configuration will be executed.

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4.8.1 Power Sequencing from POR to INIT state

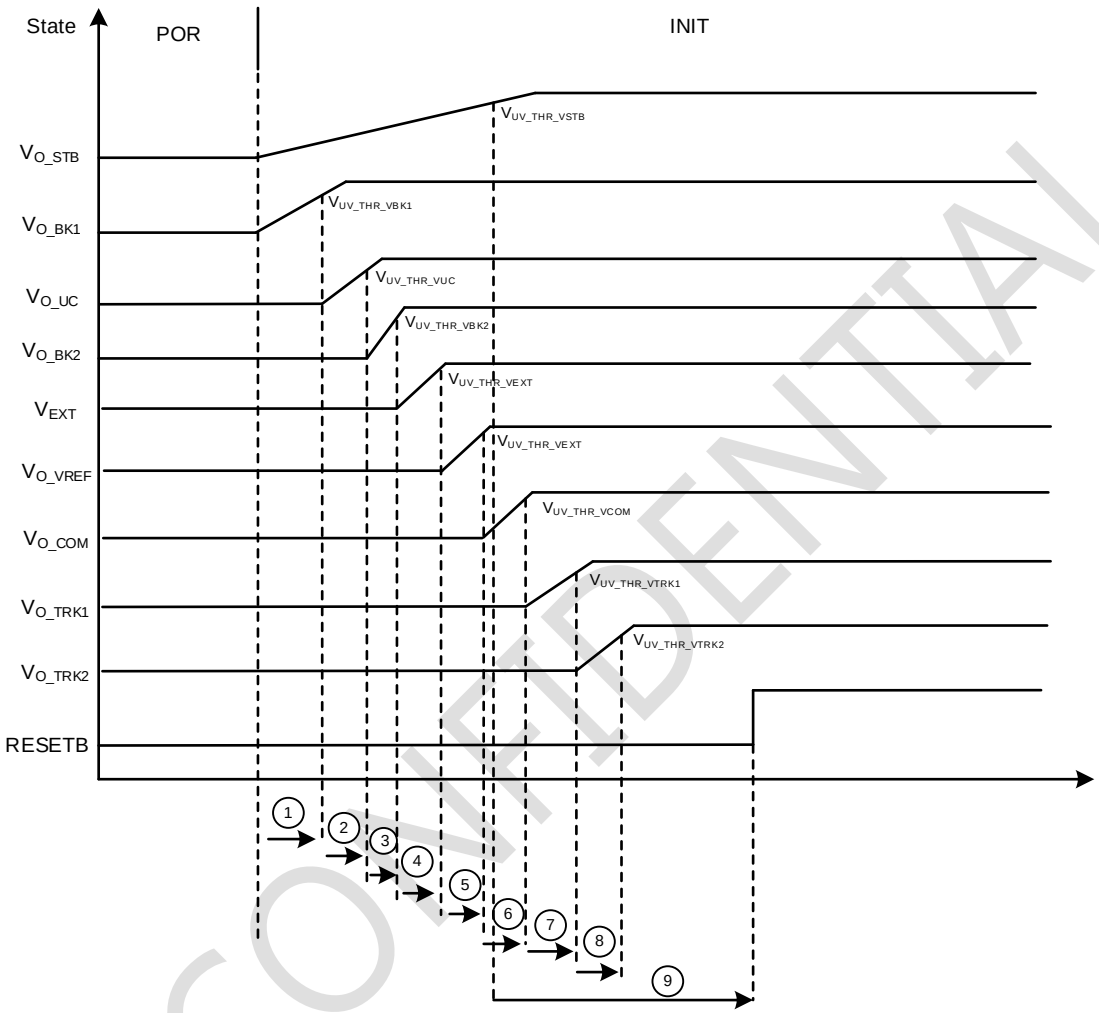

Figure 19. Power sequencing POR to INIT state

1. After POR is released the standby regulator and the pre regulator start to operate.

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VO_COM, VO_TRK1, VO_TRK2), over and under voltage are indicated by an interrupt.

• For the internal supply voltages, over and under voltage are indicated by the hardware reset pin RESETB. In case of an over or under voltage, pin RESETB is pulled to low.

Table1 Indication Pin Matrix

Regulators	OV Indication Pin	UV Indication Pin	STG Indication Pin
VO_STB	RESETB	RESETB	RESETB
VO_UC	RESETB	RESETB	RESETB
VO_BK2	RESETB	RESETB	RESETB
VEXT	RESETB/INTB selectable	RESETB/INTB selectable	RESETB/INTB selectable
VO_BK1	RESETB	INTB	RESETB
VO_COM	INTB	INTB	INTB
VO_VREF	RESETB/INTB selectable	INTB	INTB
VO_TRK1	INTB	INTB	INTB
VO_TRK2	INTB	INTB	INTB
VSUP	RESETB/INTB selectable	RESETB	NA
VCC	RESETB	RESETB	NA
Bandgap1,2	INTB	INTB	NA

5.2 Shutdown Function

A short to ground detection time t_{STG} at the pre regulator output is only active during the power sequence in INIT state. If the output voltage of the pre regulator should not be within the specified limits within a certain time frame, the device will move into FAILSAFE state. There will be no reaction on a detected short to ground once the VO_BK1 is in a valid range after crossing the first time its UV threshold. If the output voltage of the pre regulator should be too low in other cases, the behavior of the device will depend on the voltage monitoring of the post regulators.

The detection of an over voltage at output voltages VO_UC, VEXT, VO_STB, VO_VREF, VO_BK2 or VO_BK1 will shut down all regulators to protect the loads from harm or destruction and moves the device to FAILSAFE.

The detection of an over voltage at output voltages VO_COM, VO_TRK1, VO_TRK2 will shut down the related regulator to protect the loads from harm or destruction and generate an interrupt event.

If the detected under voltage at output voltages VO_UC, VEXT, VO_BK2 or VO_STB should be present for more than the short to ground detection time t_{STG}, all regulators will shut down to protect themselves and the chip from over heating and move the device to FAILSAFE.

If the detected under voltage at output voltages VO_VREF, VO_COM, VO_TRK1, VO_TRK2 should be present for more than the short to ground detection time t_{STG}, the related regulator will shut down to protect himself and the chip from over heating and generate an interrupt event.

The detection of an over voltage or under voltage at power supply voltage VSUP, internal supply voltage VCC will shut down all regulators.

Table2 Shutdown Matrix

Output	OV	UV	STG
VO_STB	All regulators shut down	No shut down	All regulators shut down
VO_UC	All regulators shut down	No shut down	All regulators shut down
VO_BK2	All regulators shut down	No shut down	All regulators shut down
VEXT	All regulators shut down/No shutdown, selectable;Assert EN_EXT	No shut down	All regulators shut down/No shutdown, selectable;Assert EN_EXT
VO_BK1	All regulators shut down	No shut down	All regulators shut down
VO_COM	VO_COM shutdown	No shut down	VO_COM shutdown
VO_VREF	All regulators shut down/No shutdown, selectable	No shut down	Related regulators shut down
VO_TRK1	VO_TRK1 shutdown	No shut down	VO_TRK1 shutdown
VO_TRK2	VO_TRK2 shutdown	No shut down	VO_TRK2 shutdown
VSUP	All regulators shut down/No shutdown, selectable	All regulators shut down	NA

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VCC	All regulators shut down	All regulators shut down	NA

5.3 Reset Function

The reset generator starts to operate as soon as the internal POR is released.
It is called a “Soft Reset” if pin RESETB goes low, but the pre and post regulator output voltages are not switched off.
It is called a “Hard Reset” if pin RESETB goes low and the post regulator output voltages are switched off. The power sequencing will be restarted after a delay of t_{SDT}.(Applicable to the second initialization timeout in a row).
The reset output pin RESETB is an open drain structure. As soon as a reset condition occurs, the RESETB pin is pulled low. An internal pull up current is pulling the output towards VO_UC.
The contribution of regulators to reset is shown in Table1. Besides, IBIAS monitoring is contributing to trigger a reset. The IBIAS monitor fault is stored in a status bit (**BIASHI** or **BIASLOW**).

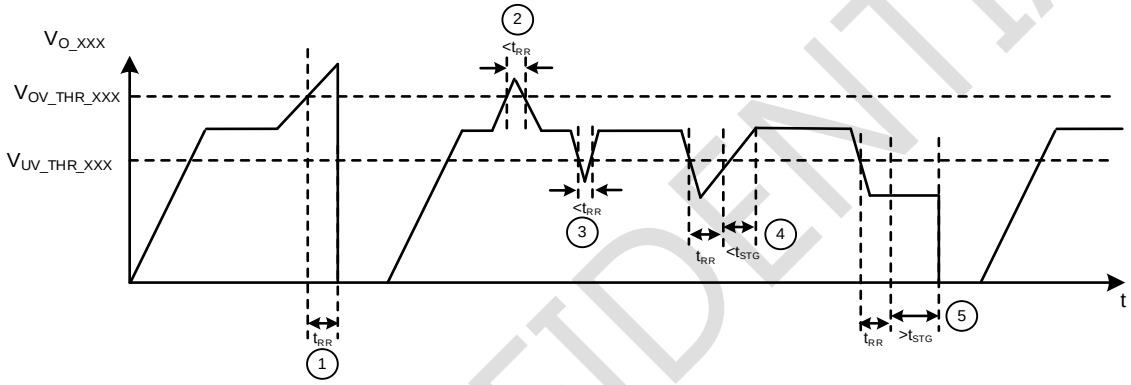

Figure 22. Timing diagram hardware reset signal RESETB for output voltages

1. Voltage exceeds OV threshold and last for longer than $t_{RR,}$ OV event is triggered.

2. Voltage exceeds OV threshold but last for shorter than t_{RR}, OV event is not triggered.

3. Voltage falls below UV threshold but last for shorter than t_{RR}, UV event is not triggered.

4. Voltage falls below UV threshold and last for longer than t_{RR}, UV event is triggered. After UV event is triggered, voltage still lower than UV threshold but last for shorter than t_{STG}, STG event is not triggered.

5.Voltage falls below UV threshold and last for longer than t_{RR}, UV event is triggered. After UV event is triggered, voltage still lower than UV threshold and last for longer than t_{STG}, STG event is triggered.

5.4 Interrupt Function

The interrupt generator starts to operate as soon as the internal POR is released.
Th
VO_COM, VO_TRK1 and VO_TRK2, the pre regulator output voltage VO_BK1

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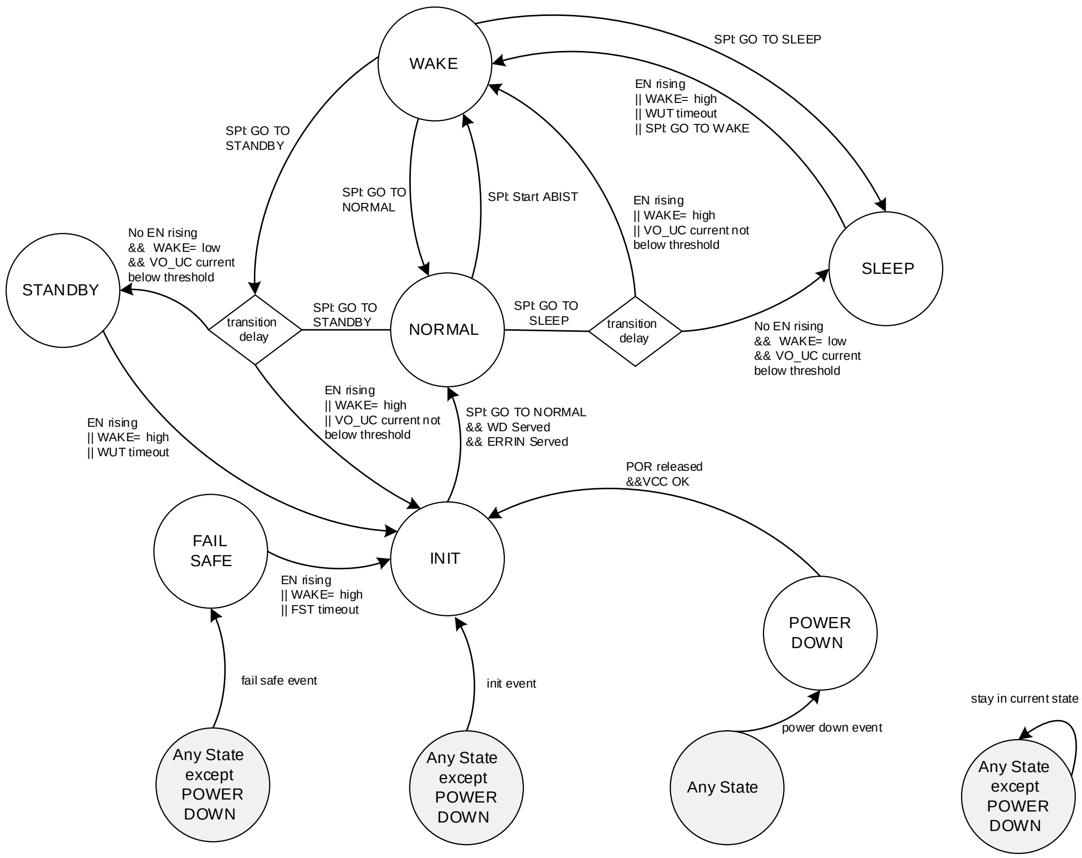

fail safe event y
- VO_UC: OV,STG,TSD
- VO_BK2: OV,STG,TSD
- VMON : OV,STG
- VO_STB OV,STG
- VO_VREF: OV
- VO_BK1: OV,STG,TSD
- VSUP: OV(except for STANDBY)
- Three initialization failures consecutively
- BIAS-current monitor
- TSD of monitoring block
- Internal error
- RESETB monitoring error

init safe event y
- VO_UC: UV
- VO_BK2: UV
- VMON : UV
- VO_STB UV
- WD Error Counter (WWD /FWD) overflow
- Error Monitoring triggered
- INIT timer expired
- CRG error

power down event y
- Internal Supplies : UV,OV
- VSUP: UV shutdown

stay in current state event y
- VO_VREF:UV, STG,OC
- VO_TRKx OV,UV, STG
- VO_COM:OV, UV ,STG,TSD
- VO_BK1: UV
- VO_STB OC
- WD Error Counter (WWD /FWD) increased
- Error Monitoring Recovery delay time active
- TSD prewarning
- Comp BG 1 <-> BG2 > 4%
- SPI communication fault

7.2 Detailed Operating States

6PTd (7)Tj 7.21(P)OWER D004 6[(ta)5t1906(-8.1429 T9)Tcta 9he de [(ta)0.v)4-1.2(a)-7c9 (069 Tcta)0. .2(a)-7s

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SS1&SS2	LOW	Both safe state signals are LOW and the application is in safe state

7.2.3 NORMAL state

In NORMAL-
resetblock and safe state control) are
wakeup timer via SPI command for this state.

Table 5 NORMAL Operation State

Block/Function	Status	Description
LDO_STB	SELECTABLE	The LDO_STB may be switched on or off by SPI command.
HV Buck1	ON	• The HV Buck1 is on • The boost is active depending on the input voltage and this option is selected by pin EN_BST.
/ ' 2 B &	ON	The is on
LV Buck2	ON	The LV Buck2 is on
External Post Regulator	ADJUSTED	The External Post Regulator is switched ON or OFF depending on pin EN_EXT
LDO_COM	SELECTABLE	The LDO_COM may be switched off or on by SPI
LDO_VREF	SELECTABLE	The LDO_VREF may be switched off or on by SPI
LDO_TRK1&2	SELECTABLE	The LDO_TRK1&2 may be switched off or on by SPI
Wakeup Timer	OFF	The Wakeup Timer is off
Watchdog	SELECTABLE	The watchdogs may be configured and switched ON or OFF by SPI
ERRIN	SELECTABLE	The Error monitoring may be configured and switched ON or OFF by SPI
RESETB	HIGH	The RESETB pin is high
SS1&SS2	HIGH	Both safe state signals are high

7.2.4 STANDBY state

consumption to a minimum

when the application is not used for a long time. The application is in a safe state.

Table 6 STANDBY Operation State

Block/Function	Status	Description
LDO_STB	SELECTABLE	The LDO_STB may be switched on or off depending on its configuration.
HV Buck1	OFF	The HV Buck1 is off
/ ' 2 B &	OFF	The is off
LV Buck2	OFF	The LV Buck2 is off
External Post Regulator	OFF	The External Post Regulator is off
LDO_COM	OFF	The LDO_COM is off
LDO_VREF	OFF	The LDO_VREF B is off
LDO_TRK1&2	OFF	The LDO_TRK1&2 is off

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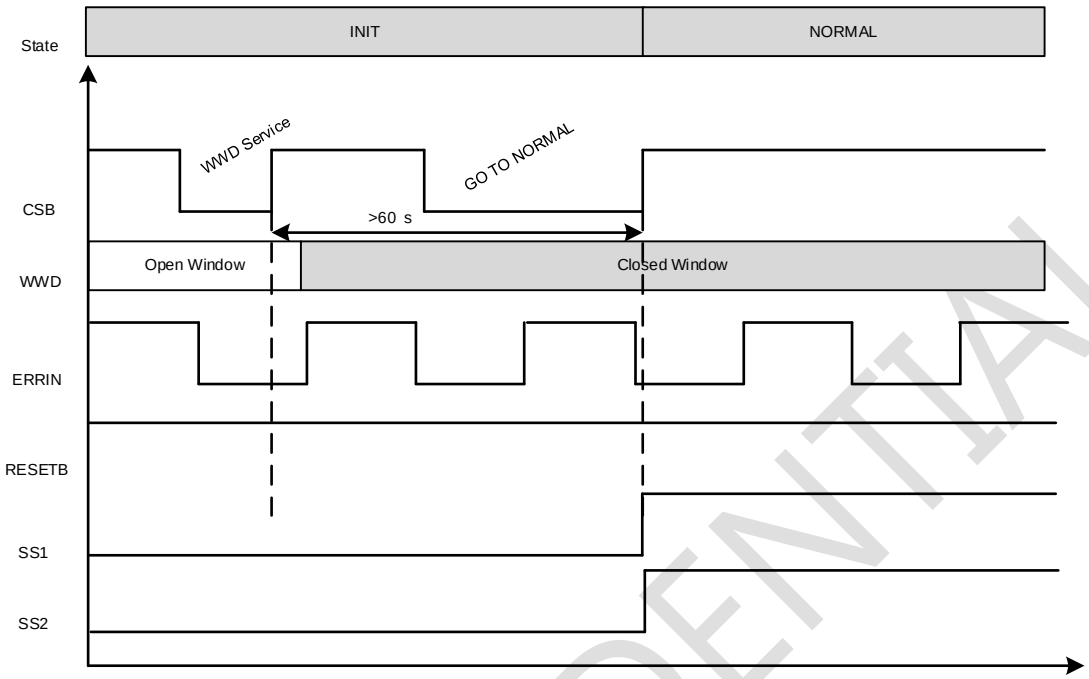

Figure 23. Transition from INIT to NORMAL state

• A valid SPI command “Go to NORMAL” (valid with chip select high at pin CSB) will move the device from INIT state to NORMAL state.
• Reset pin RESETB stays HIGH as the post regulators are already active in INIT state.
• With the positive edge of chip select high (at pin CSB) the safe state signals SS1 and SS2 are pulled to HIGH at same time. (Internal reaction time for the safe state outputs up to 30µs has to be considered)

7.3.3 NORMAL WSLEEP State

Prerequisites:

• Transition delay timer t_{TR_DEL} needs to be configured or default is used.

Triggering Events:
• State transition is only initiated by the SPI command “Go to SLEEP”.
Exceptions:
• If a valid EN (edge) or WAKE (level) signal is detected in the transition state to SLEEP state, the device will move to the WAKE state and send an interrupt (at pin INTB)

ransition delay timer t_{TR_DEL} has expired, the device will move to the WAKE state and send an interrupt (at pin INTB)

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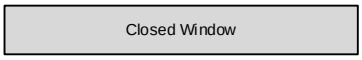

CS 0 l.09 468 -0.2.114 468-0.2.114 9.114 4 -27h/Top] W W n-/CS0 CS 0 SCN .01 w 1 j 1 J 3.202 -8.842 1.85 -0.2456 re S0 Q

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• none
Triggering Events:
• SPI command “Go to WAKE”.
• Valid Wake-up signal (EN or WAKE).

• Wake-up timer expired, if enabled
Exceptions:
• none

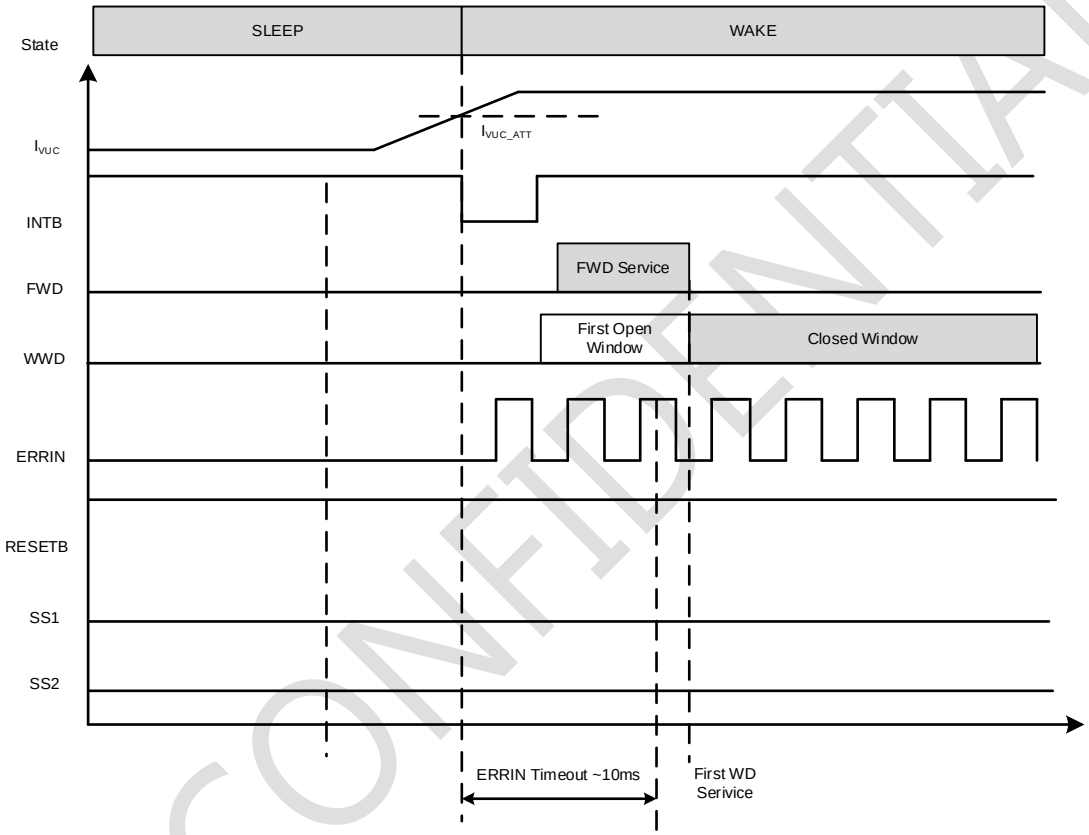

Figure 25. Transition from SLEEP to WAKE state

• The state transition is completed without a transition time and is indicated by an interrupt at pin INTB. The triggering event for the transition from SLEEP can be read from the status register **WKSF**.
• All three monitoring functions (window watchdog, functional watchdog and error monitoring) will recover to the condition active or inactive (switched off) as they were in the NORMAL state previous to the SLEEP state.
• The configuration of the LDOs will recover to the condition active or inactive (switched off) as they were in the NORMAL state previous to the SLEEP state.
• In case the window watchdog was active in the previous NORMAL state, with the negative edge of interrupt signal (at pin INTB) the window watchdog will open the first Open Window, the time of this first Open Window depends on the configured cycle time and is 600 ms (**WDCYC** = 1) or 60 ms (**WDCYC** = 0) (if the window watchdog has not been active in SLEEP state) and requires service. If the window watchdog has been active in SLEEP state continuos service is mandatory.
• In case the functional watchdog was active in the previous NORMAL state, with the negative edge of interrupt signal (at pin INTB) the functional watchdog will start the heartbeat timer and require service. If the functional watchdog has been active in SLEEP state continuos service is mandatory.
• In case the ERRIN pin monitoring was active in the previous NORMAL state, with the negative edge of interrupt signal (at pin INTB) the error monitoring will become active again. Latest 10 ms after the activation a toggling signal

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(with at least three periods past) at pin ERRIN is required. If the error monitoring has been active in SLEEP state continuos toggling is mandatory.
• Reset pin RESETB stays HIGH as the post regulators are active in SLEEP state and in WAKE state.
• The safe signals SS1 and SS2 will stay LOW in SLEEP and in WAKE state.
• If a

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• Before the SPI command “Go to SLEEP” is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of CSB signal is well in between the “closed window” of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command “Go to SLEEP”
• The positive edge of chip select (pin CSB) after the SPI command “Go to SLEEP” initiates the transition. With chip select high the device leaves WAKE state and enters the transition state (to SLEEP state).
• With chip select (pin CSB) high the error monitoring (pin ERRIN) is stopped - the toggling may end with the positive edge at pin CSB. If the error monitoring should be selected to be active in SLEEP state continuos toggling is mandatory.
• The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin CSB. If one

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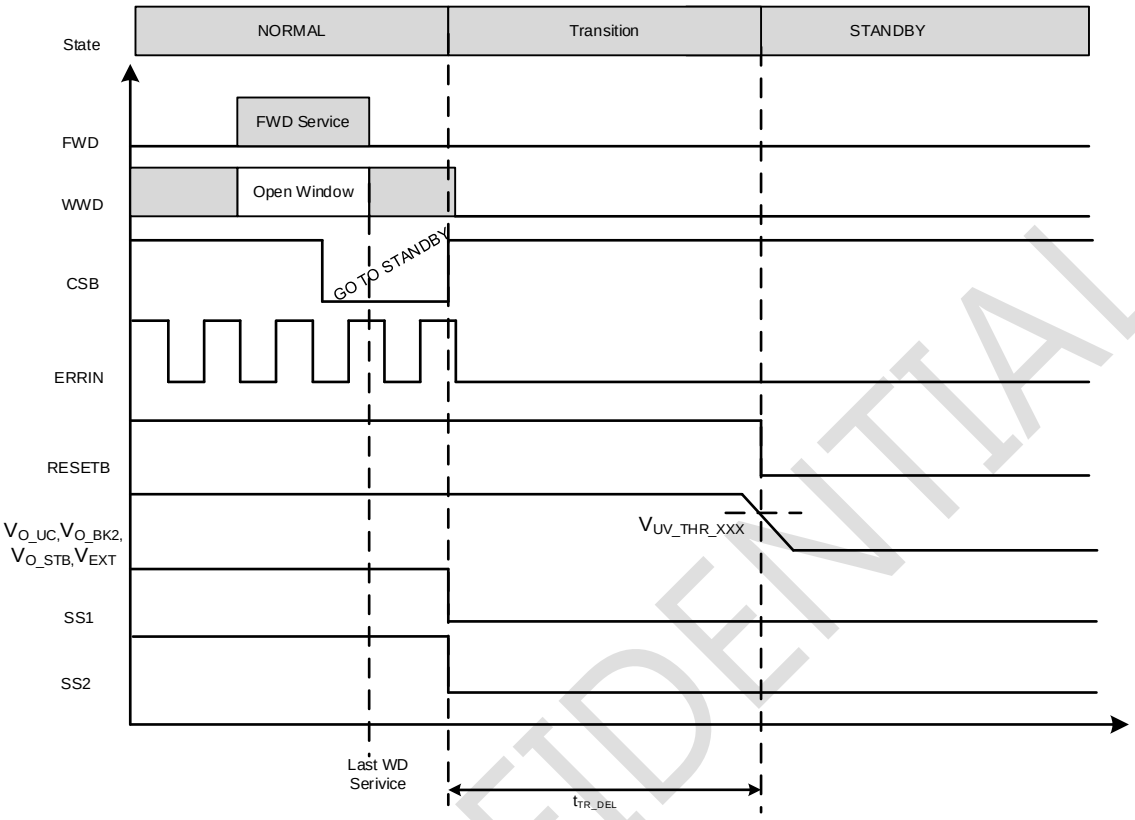

Figure 27. Transition from NORMAL to STANDBY state

• Before the SPI command “Go to STANDBY” is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of CSB signal is well in between the “closed window” of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command “Go to STANDBY”
• The positive edge of chip select (pin CSB) after the SPI command “Go to STANDBY” initiates the transition. With chip select high the safe state signals SS1 and SS2 are pulled to zero without delay between SS1 and SS2. The device leaves NORMAL state and enters the transition state (to STANDBY state). (Internal reaction time for the safe state outputs has to be considered)
• With chip select (pin CSB) high the error monitoring (pin ERRIN) is stopped - the toggling may end with the positive edge at pin CSB.
• The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin CSB.
• With a successful transition from NORMAL to STANDBY state the RESETB is pulled to LOW after the transition time after chip select (pin CSB) going high.
• All pre regulators and all post regulators (with the exception of the standby LDO - it may be ON or OFF in STANDBY state) are switched off at the point when the transition is completed after the RESETB is pulled low.
• In case the absolute transition timer is selected, the device moves from transition state to STANDBY state after the transition delay time t_{TR_DEL}. The transition time t_{TR_DEL}

current monitor is selected for the transition, the device moves from transition state to threshold

before the transition delay timer t_{TR_DEL} has expired.

7.3.7 STANDBY WINIT State

Prerequisites:
• none
Triggering Events:

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• Valid EN (edge) or WAKE (level) signal.
• Wake-up timer expired, if enabled
Exceptions:
• none

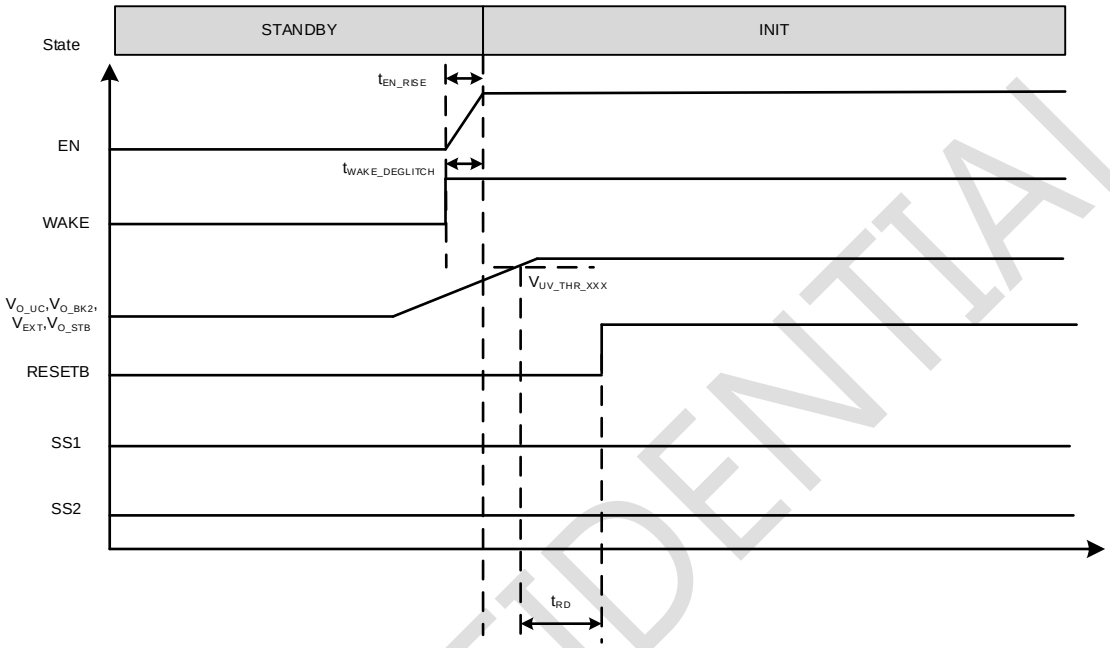

Figure 28. Transition from STANDBY to INIT state

• All pre regulators and all post regulators are switched on according to the power sequencing, except the LDO_STB is kept ON or OFF according to its configuration (simplified in figure above).
• The power on reset delay time is started as soon as the latest of the VO_UC, VO_BK2, or VEXT (if enabled) crosses the related under voltage reset threshold $V_{UV\_THR\_XXX}$ on the way up.
• After the power on reset delay time has expired the RESETB is set to HIGH.
• The safe signals SS1 and SS2 will stay LOW in STANDBY state and in INIT state.

7.3.8 WAKE WNORMAL State

Prerequisites:
• The activated supervision functions (e.g. window watchdog, functional watchdog, ERR pin monitoring) need to be serviced at least once (minimum 3 periods for ERR monitoring) in the active WAKE state, if they are restarted/reinitialized in WAKE state (e.g. watchdog being inactive in previous SLEEP state)
Triggering Events:
• State transition is only initiated by the SPI command “Go to NORMAL”.
Exceptions:
• none

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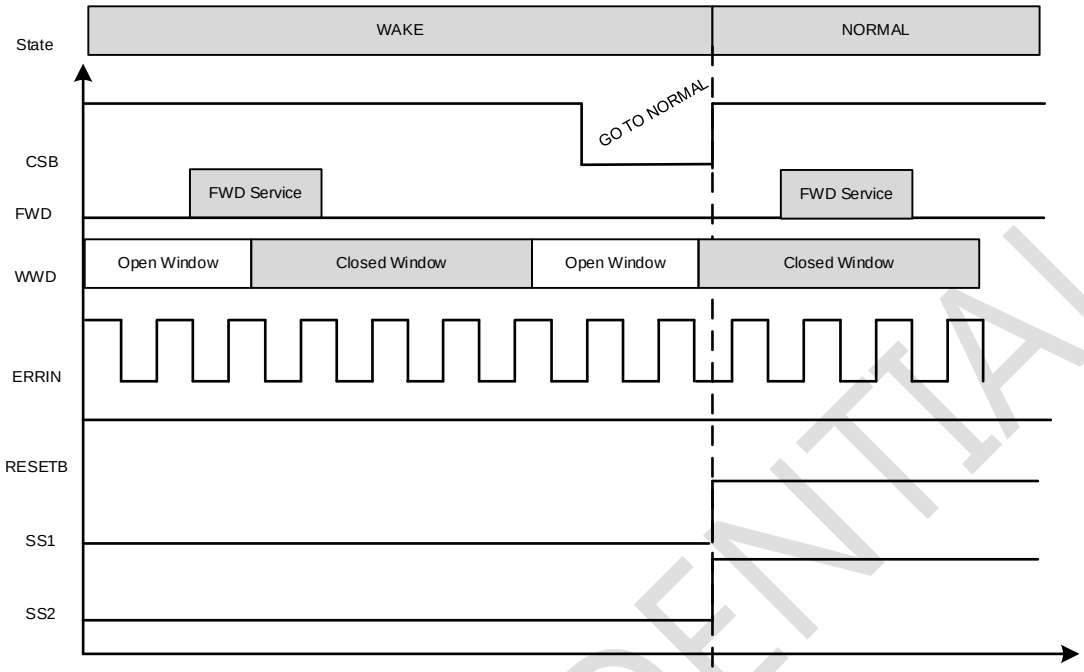

Figure 29. Transition from WAKE to NORMAL state

• The enable signal will be disregarded. A valid enable (edge) signal will not move the device from WAKE to NORMAL state.
• The state of wake signal will be disregarded. A valid wake (level) signal will not move the device from WAKE to NORMAL state.
• The window watchdog (if active in WAKE state) will require continuos service - not synchronized to the transition from WAKE state to NORMAL state.
• The functional watchdog (if active in WAKE state) will require continuos service - not synchronized to the transition from WAKE state to NORMAL state.
• The error monitoring (at pin ERRIN) (if active in WAKE state) will require a continuos toggling signal – not synchronized to the transition from WAKE state to NORMAL state - but minimum 3 periods detected to enter accept the movement into NORMAL state.
• Reset pin RESETB stays HIGH as the post regulators are active in WAKE state and in NORMAL state.
• With the positive edge of chip select high (at pin CSB) the safe state signals SS1 and SS2 are pulled to HIGH at same time. (Internal reaction time for the safe state outputs has to be considered)

7.3.9 WAKE W**STANDBY State**

Prerequisites:

transition timer.

• Transition timer needs to be configured or default is used.

Triggering Events:

• State transition is only initiated by the SPI command “Go to STANDBY”.

Exceptions:

• If a valid EN (edge) or WAKE (level) signal is detected in the transition state to STANDBY state, the device will move to the INIT state and a reset is generated.

controller is not below the selected current threshold before the transition timer has expired, the device will move to the INIT state and a reset is generated.

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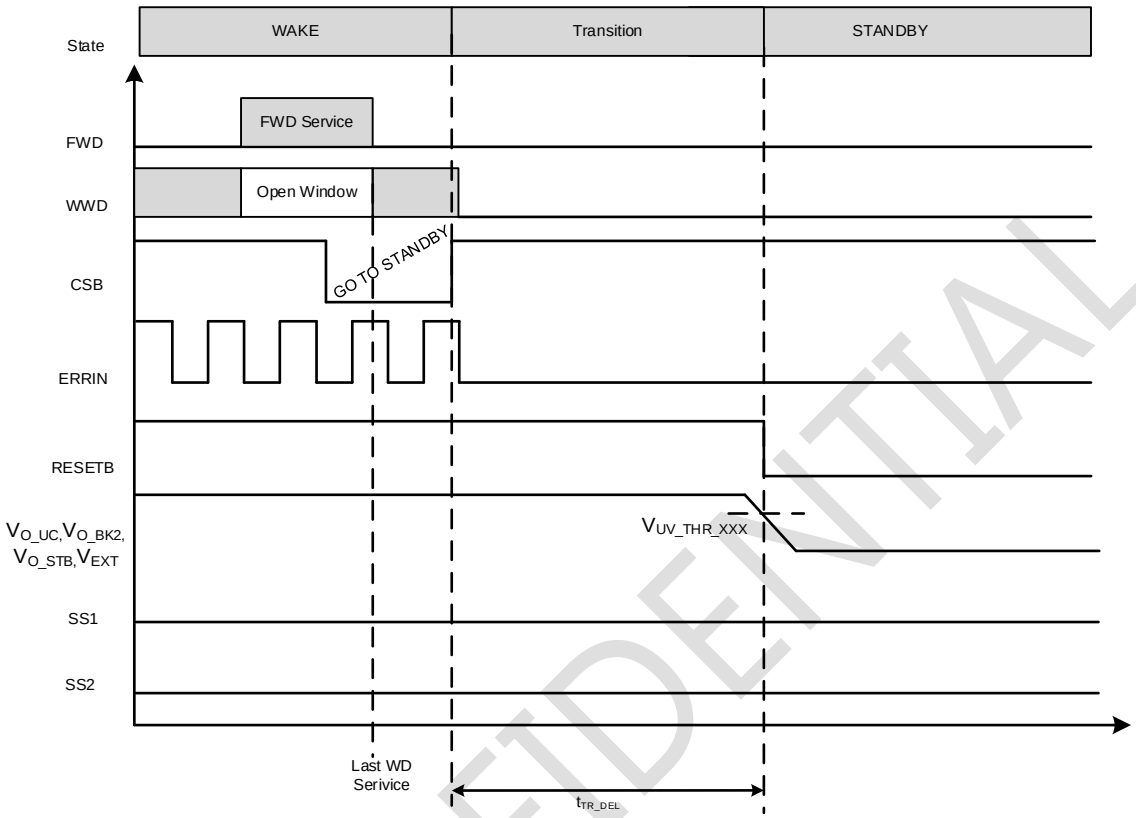

Figure 30. Transition from WAKE to STANDBY state

• Before the SPI command “Go to STANDBY” is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of CSB signal is well in between the “closed window” of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command “Go to STANDBY”
• The positive edge of chip select (pin CSB) after the SPI command “Go to STANDBY” initiates the transition. In the WAKE state the safe state signals SS1 and SS2 are LOW and will be kept LOW for the transition to STANDBY. The device leaves WAKE state and enters the transition state (to STANDBY state).
• With chip select (pin CSB) high the error monitoring (pin ERRIN) is stopped - the toggling may end with the positive edge at pin CSB.
• The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin CSB.
• With a successful transition from WAKE to STANDBY state the reset (RESETB) is pulled to LOW after the transition time after chip select (pin CSB) going high.
• All pre regulators and all post regulators (with the exception of the standby LDO - it may be ON or OFF in STANDBY state) are switched off at the point when the transition is completed after the reset (RESETB) is pulled low.
• In case the absolute transition timer is selected, the device moves from transition state to STANDBY state after the transition time t_{TR_DEL}. The transition time t_{TR_DEL}

monitor is selected for the transition, the device moves from transition state to threshold

before the transition delay timer t_{TR_DEL} has expired.

7.3.10 FAILSAFE WINIT State

Prerequisites:
• FAILSAFE timer has expired.

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over movement to FAILSAFE which takes precedence over movement to INIT.
The move to INIT, FAILSAFE and POWERDOWN errors are named “error triggered state transitions” in this document.

7.4.1 INTERRUPT Events

The following failures will not trigger a movement of the device to another state by themselves, but will indicate the failure by an interrupt event:

• Detection of under voltage or a short to ground or overload detection at voltage reference

• Detection of over voltage, under voltage or a short to ground at trackers 1 or 2

• Detection of over voltage, under voltage, a short to ground or thermal shutdown at LDO_COM

• Detection of under voltage at pre regulator.

• Detection of overload at standby regulator

• Increase of window/functional watchdog status counter, but actual value still stays below the threshold

• Error monitoring recovery delay time is active and ERR signal stops toggling.

• OM)

• Bandgap monitoring: If the deviation between both bandgaps is larger than 4%

The interrupt may not be visible on the INTB pin in STANDBY and FAILSAFE state due to microcontroller supplies being switched off. The event is stored in the status flags (IF, SYSSF, MONSF0, MONSF1, MONSF2, OTWRNSF, OTFAIL).

7.4.2 INIT Events

The following failures will bring the device from any state to INIT state:
• Detection of under voltage at LDO_UC, VEXT. or LDO_STB
• Detection of window/functional watchdog status counter overflow
• Stop of error signal detected (immediate reaction mode) or stop or error signal detected for more than recovery delay time (recovery mode)
• One or two consecutive expires of the INIT timer (configuration in INIT state failed)

z **Transition into INIT State due to INIT timer expired for the first time**

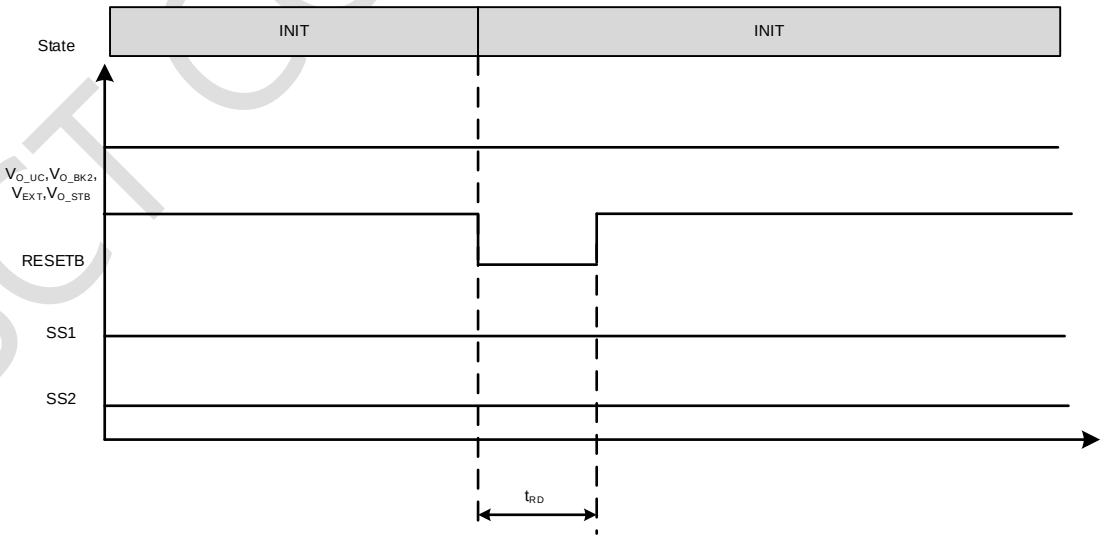

Figure 32. Transition from INIT to INIT state - first movement

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• Detection of over voltage at VO_VREF
• Detection of over voltage, short to ground1) (only during startup phase in INIT state) or thermal shutdown at pre regulator
• Three consecutive initialization failures(e.g. configuration in INIT state failed)
• A BIAS current monitor failure
• A over temperature shutdown due to exceeded temperature in the monitoring block.
• A fuse selection monitor failure
• An over voltage at the supply pins (VSUP) will trigger the overvoltage protection and move the device into FAILSAFE-state (except for STANDBY state)

z **Transition into FAILSAFE State due to STG**

Description:

• O_UC, VO_BK2,VO_STB or VEXT as shown in the figure will initiate the transition from NORMAL/SLEEP/INIT/WAKE into INIT state. (please refer to previous chapter Transition into INIT state)

• Pin RESETB will be pulled to LOW as soon as the under voltage is detected (at one or more of the regulators mentioned above - whichever is the first)

• The safe state signal SS1 will be pulled to LOW together with pin RESETB going to low

• If the short to ground maintains for longer than the short to ground detection time t_{STG} a short to ground event is detected.

• All regulators will be switched off as soon as the short to GND is detected, regardless if they are in under voltage condition or not.

• The device moves from INIT state to FAILSAFE state

• The safe state signal SS2 will be pulled to LOW together with the transition from INIT to FAILSAFE state, even if the delay time t_{SS_DLY} state, but switched off in FAILSAFE state).

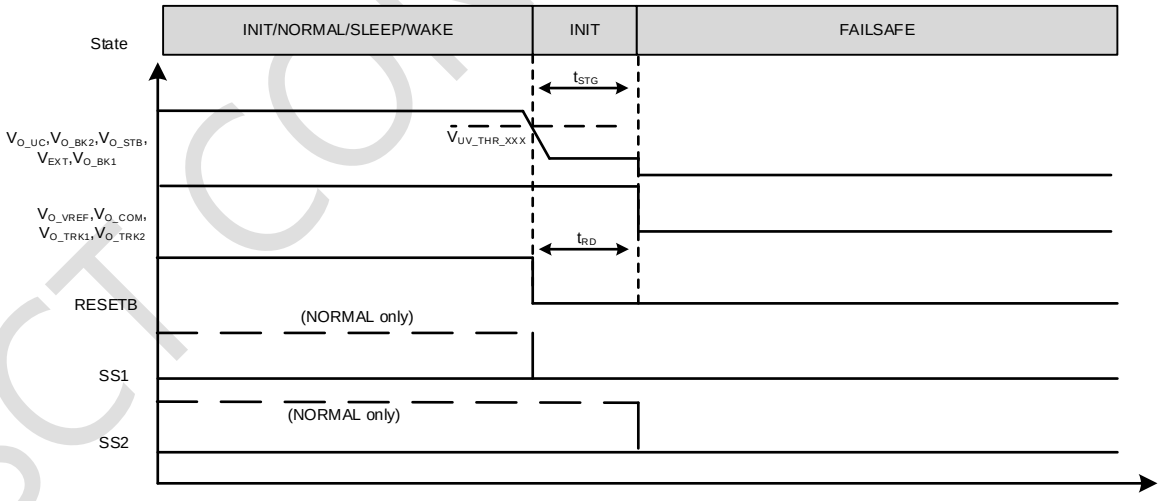

Figure 37. Transition into FAILSAFE state due to STG fault

• The device transitions from STANDBY into INIT state might be issued by an undervoltage of the VO_STB. The pin RESETB is pulled to LOW and all the outputs are enabled, except the LDO_STB will keep its configuration being ON or OFF. Disabled outputs will get switched on again. An under voltage longer than the short to ground detection time t_{STG} would lead to a transition from INIT to FAILSAFE state and all regulators will be switched off.

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the selected comparator(s) are tested. In case more than one comparator is selected, the test is performed with a fixed sequence of comparators to be tested. The completion of the test is indicated by an interrupt.
• The functionality of a comparator including its corresponding deglitching logic and the contribution to the respective safety measure can be tested. The safety measure is either the activation of the secondary safety shutdown path or the generation of an interrupt. This test is performed in a time longer than the deglitching time.
• While the device provides information about the status for the first and the second ABIST, further microcontroller cooperati shutdown path has been activated successfully (SS1/SS2 are set low) or an interrupt event has been detected

7.5.2.2 How to run the ABIST

During ABIST, servicing of the watchdog(s) and error monitoring is required to be performed according to the configuration by the microcontroller. Error in not doing so will lead to failure events in these functions and will lead to the assertion of interrupt, reset or safe state output events accordingly, which is disturbing the proper analysis of the ABIST results. Optionally watchdog functionality and/or error monitoring can be disabled during ABIST operation via a protected register access. In this case, no servicing is required.
During a performed ABIST including the deglitching logic the FLAG registers (**SYSFAIL**, **INITERR**, **IF**) as well as the status information (**MONSF1**, **MONSF2**, **MONSF3**) are triggered and updated by out of range conditions caused by the ABIST functionality, which has to be considered beside the results provided in the ABIST related registers (**ABIST_CTRL0** to **ABIST_SELECT2**).
During the time, when the ABIST is performed by internal hardware, the assertion of RESETB due to the occurrence of any event which is supposed to trigger the respective action and is part of the logic which is affected by the ABIST control is blocked. In addition, the state machine will not change its state according to the reaction on detected faults. In case an ABIST contributing to the secondary safety shutdown path is started and the device is in NORMAL state, the state machine will move from NORMAL to WAKE state.
Furthermore, all voltages will be kept enabled regardless of any out of range detection caused by ABIST itself. The test of a single functionality is basically always performed in the same way:

Accordingly, configurable LDO's have to be enabled before they can be tested. On the other hand the ABIST test on a comparator which is not used by the system is not required to be performed.
• The comparators to be tested shall be selected by setting the individual bit(s) in the respective register(s) (**ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**). For this selection it is necessary to differentiate by the contribution to the different safety measure.
• The microcontroller shall configure the register **ABIST_CTRL0** according to the functionality to be tested. The configuration consist of the tested safety measure (**ABIST_CTRL0**.**INT**), the tested area/coverage by the ABIST (**ABIST_CTRL0**.**PATH**) and the configuration whether a sequence or a single comparator shall be tested (**ABIST_CTRL0**.**SINGLE**).
• The microcontroller shall set the global ABIST start bit (**ABIST_CTRL0**.**START**) to start the ABIST.

performed.
Upon completion of the selected ABIST operation(s) the start bit is cleared and an interrupt event is generated.
• Each bit which has been set to select the test of a dedicated comparator (**ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**) is cleared once a successful ABIST operation has been performed on the particular comparator. Each bit which has been set to select the test of a dedicated comparator is kept unchanged if the ABIST operation on this particular comparator has not been performed successfully.
determine which comparator failed in case the ABIST status information shows a failing ABIST operation.

7.5.2.3 Testing the comparator logic only

During the ABIST operation the comparators are triggered by the ABIST controller for a time shorter than the internal deglitching time t_{RR} (reset reaction time). A properly working comparator signals an out of range condition to its output for the time the failure condition is applied.
The provided information of each comparator is checked against the expected value. If the comparator output value matches the expected value this is considered as a passing test by the ABIST controller. If any of the provided output values do not match the expected value, this is considered as a failing test. The general result of the ABIST is provided by the **STATUS** in the register **ABIST_CTRL0**. The detailed result for each selected comparator can be checked by the registers **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**. In case the previously

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selected bits are reset after the test is finished, it can be considered as pass. A bit which is still set, would indicated the failing comparator(s), that makes the overall **STATUS** to be failed.
Accordingly the maximum selection(1) (including possible ones) for the comparator test would be the following:
Secondary safety shutdown path (SS1/2) related:
• **ABIST_SELECT0** : 00101111b (2Fh)
• **ABIST_SELECT1** : 00001110b (0Eh)
• **ABIST_SELECT2** : 11001001b (C9h)
• Start of the test by **ABIST_CTRL0** : 00000001b (01h)
Interrupt (INTB) related:
• **ABIST_SELECT0** : 11010000b (D0h)
• **ABIST_SELECT1** : 11110001b (F1h)
• **ABIST_SELECT2** : 00110000b (30h)
• Start of the test by **ABIST_CTRL0** : 00001001b (09h)
This type of ABIST can be performed in the following states of the **State Machine**: INIT, NORMAL, WAKE. In case of an successful ABIST there shall be no reaction of secondary safety shutdown path SS1/2 and only an interrupt generated due to the finished ABIST (**IF**.**ABIST** set and **IF**.**MON** not set, considering cleared interrupt flags prior to the ABIST and no real failure events during the ABIST).
1) Please mind that for a test of a comparators the corresponding output has to be enabled.

7.5.2.4 Testing the comparator logic and the corresponding deglitching logic

During the ABIST operation the comparators are triggered by the the ABIST controller for a time longer than the internal deglitching time t_{RR} (reset reaction time). A properly working comparator signals an out of range condition to its output for the time the failure condition is applied. The deglitching logic will forward the failure trigger after trr and makes the device react on the recognized failure event. This reaction consists the storage of the respective monitoring failure flags and as well the triggering of the respective output function, which is either the interrupt INTB or the secondary safety shutdown path SS1/2. The reaction of the safe state outputs SS1/2 can only be observed in case the test is started in NORMAL state.
Furthermore the provided information of each deglitching logic output is checked against the expected value. If the deglitching logic output value matches the expected value this is considered as a passing test by the ABIST controller. If any of the provided output values do not match the expected value, this is considered as a failing test. The general result of the ABIST is provided by the **STATUS** in the register **ABIST_CTRL0**. The detailed result for each selected comparator can be checked by the registers **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**. In case the previously selected bits are reset after the test is finished, it can be considered as pass recognized by the ABIST controller. A bit which is still set, would indicated the failing comparator(s), that makes the overall **STATUS** to be failed.
Beside the results read from the ABIST controller related registers, the result provided in the failure/interrupt flags (**SYSFAIL**, **INITERR** and **IF**) and monitoring status flags (**MONSF1**, **MONSF2** or **MONSF3**) have to be read and checked by the microcontroller against the expected result considering the configuration set before the start of the ABIST. **INTOV** located in register **ABIST_SELECT2** cannot be tested in this way, testing of the comparator logic only is required.
The maximum selection(1) for the comparator and deglitching logic test would be the following:
Secondary safety shutdown path (SS1/2) related:
• **ABIST_SELECT0** : 00101111b (2Fh)
• **ABIST_SELECT1** : 00001110b (0Eh)
• **ABIST_SELECT2** : 11000001b (C1h)
• Start of the test by **ABIST_CTRL0** : 00000011b (03h)
Interrupt (INTB) related:
• **ABIST_SELECT0** : 11010000b (D0h)
• **ABIST_SELECT1** : 11110001b (F1h)
• **ABIST_SELECT2** : 00110000b (30h)
• Start of the test by **ABIST_CTRL0** : 00001011b (0Bh)
The analysis based on the maximum possible selection would consist the following:
Secondary safety shutdown path (SS1/2) related:
• **IF** : 01000000B (40h)
• **INITERR** : 00000100b (04h)

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• **SYSFAIL** : 00000100b (04h)
• **MONSF1** : 00101111b (2Fh)
• **MONSF2** : 00001110b (0Eh)
• **MONSF3** : 11000001b (C1h)
• Start of the test by **ABIST_CTRL0** : 00000011b (03h)
Interrupt (INTB) related:
• **IF** : 01001000b (48h)
• **INITERR** : 00000000b (00h)
• **SYSFAIL** : 00000000b (00h)
• **MONSF1** : 11010000b (D0h)
• **MONSF2** : 11110001b (F1h)
• **MONSF3** : 00110000b (30h)
• Start of the test by **ABIST_CTRL0** : 00001011b (0Bh)
This type of ABIST can be performed in the following states of the **State Machine**: INIT, WAKE, NORMAL. If this test is run in NORMAL state on comparators contributing to the secondary safety shutdown path the device will switch low the safe state outputs SS1/2 and the **State Machine** will move to WAKE state, without triggering a reset. It has to be considered that testing the complete monitoring chain till the respective output (SS1/2 or INTB) in this way will cover only the first comparator in the sequence, as this one will trigger the output reaction.
If this test is run in INIT or WAKE state, contribution to activation of the secondary safety shutdown path cannot be tested. The system is in a safe state already and the secondary safety shutdown path is already activated. In any way the proper behavior of the secondary shutdown path as well as the interrupt signal needs to be checked by the microcontroller.

7.5.2.5 Testing the complete monitoring chain (comparators, deglitching and output)

The testing of the complete monitoring chain from the comparator till the respective output function has to be divided into the two functions available in SCT61490S. First the secondary safety shutdown path called SS1/2 for severe microcontroller related failure events and secondly the interrupt function INTB for peripheral related failure events in terms of voltage and current monitoring.
• **Testing the activation of the secondary safety shutdown path:**
To test the activation of the secondary safety shutdown path, the device has to be brought into NORMAL state. The -activated successfully (SS1/2 high).
Once in NORMAL state a single comparator contributing to the secondary safety shutdown path shall be selected. A single bit ('x') has to be set for a corresponding comparator in registers **ABIST_SELECT0** (00x0xxxxb), **ABIST_SELECT1** (0000xxx0b) or **ABIST_SELECT2** (xx00000xb). A randomized selection by the microcontroller ensures maximum coverage of the contributions to the secondary safety shutdown path. Then a single comparator ABIST operation on the full path of the secondary safety shutdown path needs to be started (register **ABIST_CTRL0**: 00000111b (07h)). Upon completion of the requested ABIST operation the device will autonomously move into WAKE state and an interrupt event is generated. The interrupt event will indicate the completion of the ABIST (**IF**.**ABIST**). Furthermore the respective monitoring failure flag for the selected comparator will be set (either **INITERR**.**VMONF** for "**Move to INIT State**" failures or **SYSFAIL**.**VMONF** for "**Move to FAILSAFE State**" failures) which has to be checked and cleared by the microcontroller.
The secondary safety shutdown path shall be
activation of the secondary safety shutdown path. If SS2 delay is enabled, this delay will be applied when the ABIST operation is performed, i.e. the activation of the shutdown path connected to SS2 will be delayed according to the programmed value for failure cases not leading to FAILSAFE.
ABIST_CTRL0.**STATUS**), the respective monitoring status flag (**MONSF1**, **MONSF2** or **MONSF3**) to be set according to the previous selection and **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2** bits to be cleared.
Furthermore, the microcontroller has to proceed with the following steps to check the safe state control and the safe state outputs:
• Check that the secondary safety shutdown path has been activated successfully (SS1/2 low)
• Enable overvoltage trigger of the safe state control (set **ABIST_CTRL1**.

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• De-select generation of toggling signal for the safe state control (reset **ABIST_CTRL1**.**ABIST_CLK_EN**)

• Disable overvoltage trigger of the safe state control (set **ABIST_CTRL1**.**OV_TRIG**)

Afterwards a test of all comparators which contribute to the activation of the secondary safety shutdown path shall be configured and started.

• **Testing the generation of an interrupt event:**

The test of the generation of an interrupt event can be done in the states INIT, NORMAL and WAKE state. Even though it is recommended to have the application in safe state (INIT or WAKE state).

For this test first a single comparator contributing to the interrupt function shall be selected. A single bit ('x') has to be set for a corresponding comparator in registers **ABIST_SELECT0** (xx0x0000b), **ABIST_SELECT1** (xxxx000xb) or **ABIST_SELECT2** (00xx0000b). A randomized selection by the microcontroller ensures maximum coverage of the contributions to the interrupt function. Then a single comparator ABIST operation on the full path of the interrupt needs to be started (register **ABIST_CTRL0**: 00001111b (0Fh)). The artificial failure, triggered by the ABIST controller, on the selected comparator will generate an interrupt (INTB) event. It is the responsibility of the check the generation of this interrupt event on the triggered failure. As this is a test of the generation of an interrupt based on a failure event, there is no dedicated ABIST completion event, nor the **ABIST** bit in the interrupt flags will be set. Accordingly it is recommended to store the information about the started ABIST in the firmware.

After the interrupt has been generated the interrupt flag register shall be checked for the monitoring bit (**IF**.**MON**) set and the ABIST completion bit (**IF**.**ABIST**) not set.

ST operation (**ABIST_CTRL0**.**STATUS**), the respective monitoring status flag (**MONSF1**, **MONSF2** or **MONSF3**) to be set according to the previous selection and **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2** bits to be cleared.

Afterwards a test of all comparators which contribute to the interrupt generation shall be configured and started.

7.5.2.6 Abort conditions for ABIST operation

In case of an severe monitoring failure event (contribution to the secondary safety shutdown path) detected on a not selected comparator1) or a severe failure event not related to the voltage or bias current monitoring function during the proceeding of an ABIST operation on the comparators only (**ABIST_CTRL0**.**PATH** not set), the device will react as it is supposed to do in normal operation. Accordingly the monitoring, reset and safe state control are reacting. Bringing the device into safe state and trigger the **State Machine** to move into FAILSAFE or INIT state. The ABIST is aborted in this case.

In case of an ABIST operation on the full path (**ABIST_CTRL0**.**PATH** set) the comparators for voltage and bias current monitoring are blind for the time of the ABIST operation. Therefore it is recommended to do the test in safe state unless it is needed to start the test in NORMAL state (e.g. test of activation of secondary safety shutdown path). Severe failure events not related to the voltage and bias current monitoring will trigger the same device reaction as in usual condtion. Bringing the device into safe state and trigger the **State Machine** to move into FAILSAFE or INIT state. The ABIST is aborted in this case.

This ABIST abort will be recorded in the register **SYSFAIL**.**ABISTERR**. The artificial failure events, that have been generated until the abort of the ABIST due to the detected real failure, will be stored as well in the monitoring registers.

7.6 Microcontroller Programming Support

The device offers a microcontroller programming support feature, that can be used to avoid periodic reset triggering due to missing triggering of the window watchdog and error monitoring within the INIT timer. The activation of the microcontroller programming support feature shall be done by pulling the PROG pin to 5 V. The voltage shall be provided earliest with the enabling of the voltage reference. Therefore it would be one option to connect the PROG pin to the output VO_VREF during microcontroller programming.

The active microcontroller programming support feature includes the following changes to the normal operation of the device:

• The INIT timer will be stopped.

• The contribution of the window watchdog failure counter overflow to the reset will be blocked.

• The contribution of the functional watchdog failure counter overflow to the reset will be blocked.

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• The contribution of the error monitoring to the reset will be blocked.

As only the contribution of the watchdogs and the error monitoring to the reset function is blocked/disconnected, the state machine and safe state control function are not affected. Accordingly an overflow of the window or functional watchdog failure counter will trigger a “Move to INIT” event, but without issuing a reset of the microcontroller.

The microcontroller programming support feature offers as well the possibility to move the device to any other state according to the state machine. E.g. in case PROG pin is high in NORMAL and there is a watchdog error counter overflow the device would move into INIT without issuing a reset.

8 Safe State Control Function

8.1 Introduction

The safe state control monitors safety related signals and controls the safe state signals SS1 and SS2.

The following description summarizes the contributors to the safe state control function and the possibilities to adjust them.

Principle of operation:

The safe state control function monitors the following inputs:

• Result of the Error Monitoring. “Error”-signal at pin ERRIN is expected to be a toggling signal. A permanent low or high signal will be detected as an error.

• Over and under voltage of the micro processor related regulators

• Result of Window Watchdog Failure Counter Threshold Comparator. Whether threshold WWO for “Invalid window watchdog triggering” has been exceeded.

• Result of Functional Watchdog Failure Counter Threshold Comparator: Whether threshold FWO for “Invalid functional watchdog triggering” has been exceeded.

• Thermal shutdown signal (TSD) for relevant events moving the device into FAILSAFE state.

• Internal clock

• SPI state transition request. A valid GoToNORMAL command triggers the signals SS1/2 to switch high in case the other boundary conditions are fulfilled. Moving the device out of NORMAL state by SPI command will switch the signals SS1 and 2 (optionally delayed by t_{SS_DLY}) to low.

The following parameters of the safe state control function are programmable via SPI, this settings can be done during INIT, NORMAL, SLEEP and WAKE state, WWD and FWD configuration and error pin configuration including disabling of individual functionality via protected register:

• Number of invalid watchdog triggers, that lead to activating SS1 and SS2: There are two watchdog trigger failure counters implemented, one for the window watchdog the other for the functional watchdog. Every counter increments by two at every invalid watchdog triggering and decrements by one at every valid watchdog triggering. (valid and invalid triggering is described in chapter functional and window watchdog). An incrementing change is indicated by an interrupt. A decrementing change is not indicated by an interrupt. The thresholds can be programmed by SPI command for each counter individually. This function might be used to test the watchdog function.

• Immediate reaction or recovery delay reaction, only related to input signal ERR: This parameter determines whether the safe state control will immediately react to an error indicated by SMU or react after a certain delay, if the error indication is still present. In recovery delay reaction the safe state control will generate an interrupt and start the programmed recovery delay time. If within this time the error should disappear (means the error signal should toggle again, before the recovery delay time has ended), the safe state control will keep the safe state output SS1/2 high. If within this time the error signal should not disappear and maintain the error indication (means the error signal should not toggle again, before the recovery delay time has ended), the safe state control will activate the safe state signals SS1 and SS2 after the recovery delay time has ended.

Immediate reaction means reaction after signal detection delay time.

• Recovery delay time t_{REC}, only related to input signal ERR: An error (violation of valid ERR signal) has to be longer than this delay time to lead to activating the safe state signals SS1 and SS2. This delay time is only active if recovery delay time mode was selected.

• Delay time t_{SS_DLY} between safe state signal 1 and safe state signal 2

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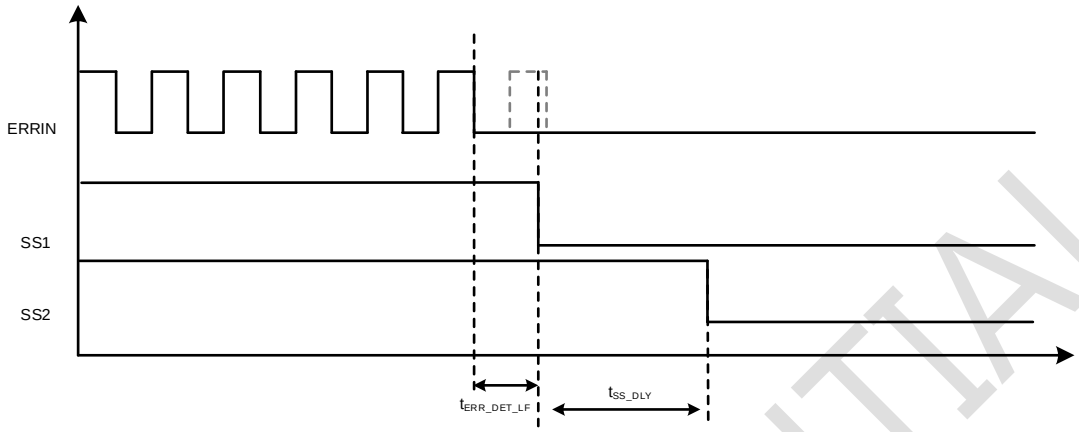


Figure 41. Flow diagram reaction on SMU signal (ERRIN signal remains low)

- **ERRIN signal remains high**

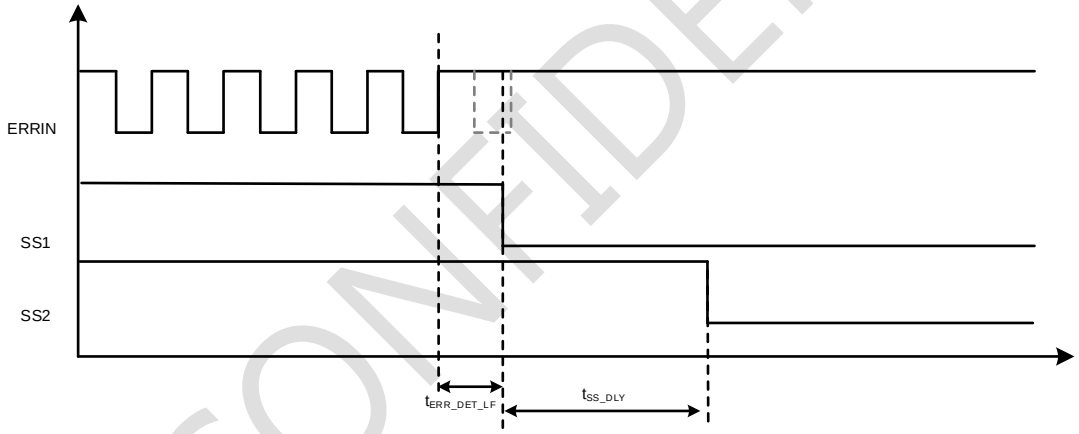
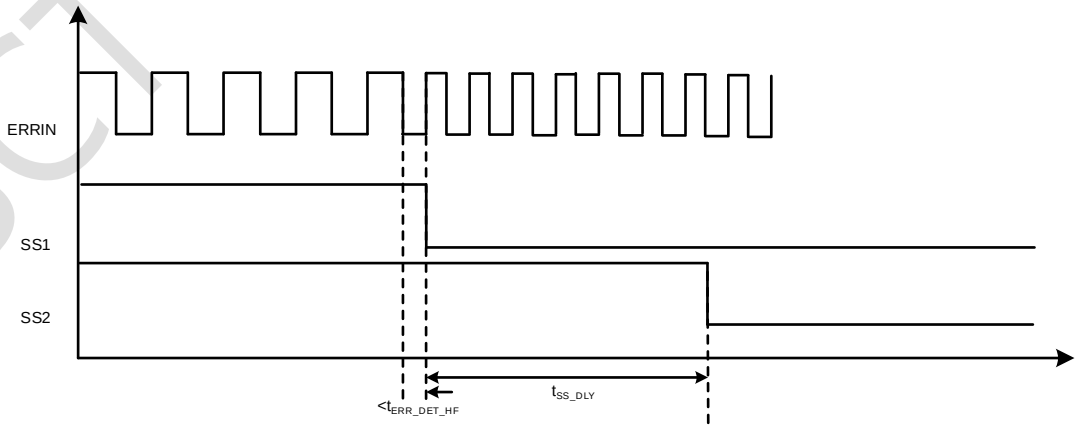


Figure 42. Flow diagram reaction on SMU signal (ERRIN signal remains high)

- **ERRIN signal frequency too high**



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• ERRIN signal too long with changing high and low times(duty cycle can vary as well)

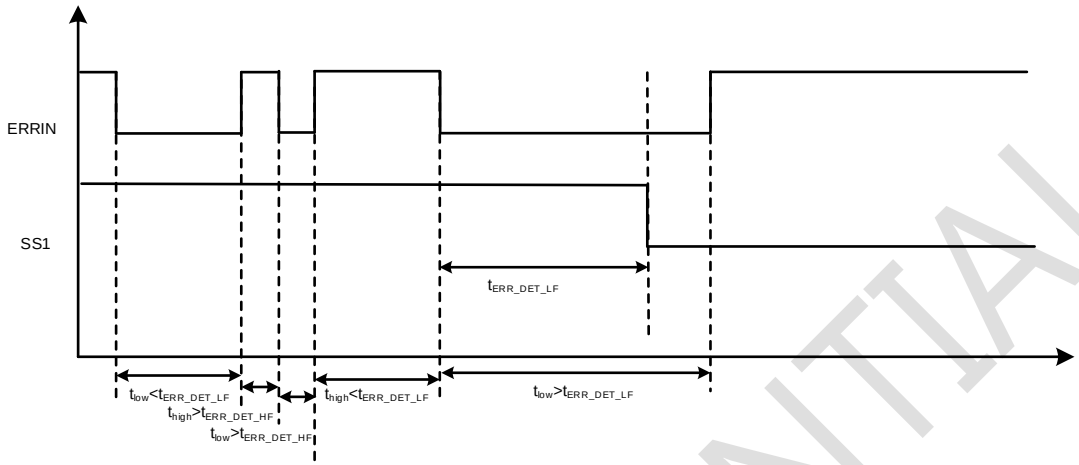

Figure 44. Flow diagram reaction on SMU signal (ERRIN signal too long)

• ERRIN signal too short with changing high and low times(duty cycle can vary as well)

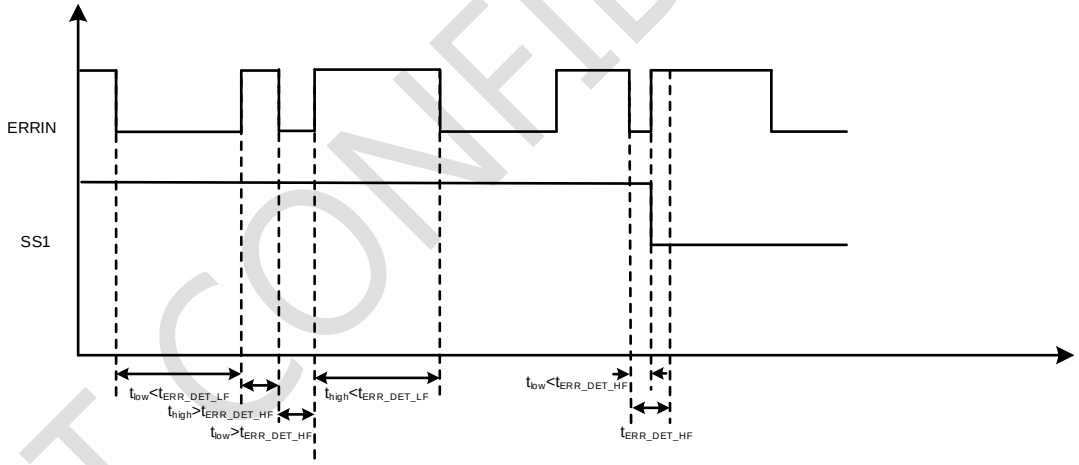

Figure 45. Flow diagram reaction on SMU signal (ERRIN signal too short)

8.2.2)

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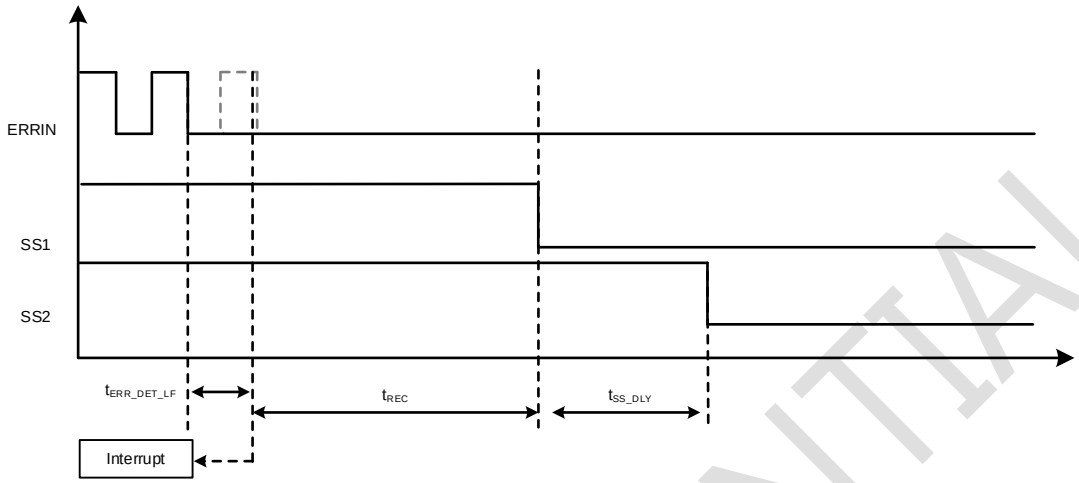

Figure 46. Flow diagram reaction on SMU signal, error longer than recovery delay time

- **ERRIN signal frequency too high**

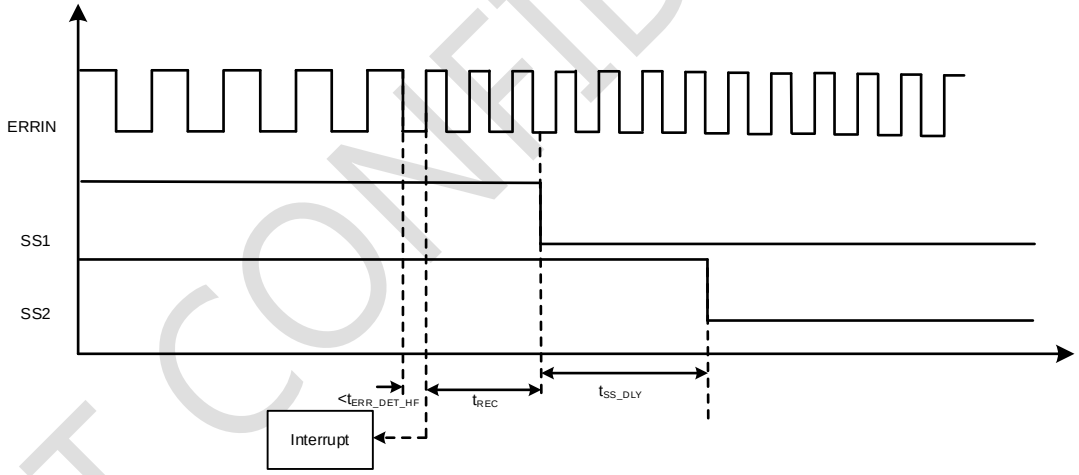

Figure 47. Flow diagram reaction on SMU signal, error longer than recovery delay time (ERRIN signal frequency too high)

- **ERRIN remains low or high and error shorter than recovery delay time**

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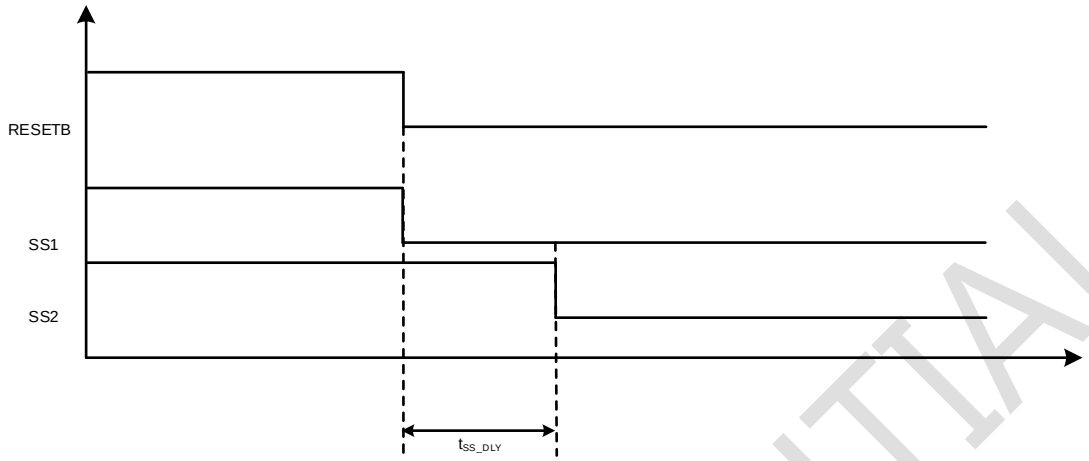

Figure 50. Flow diagram reaction on an error triggered state transition- soft reset

• **Hard reset**

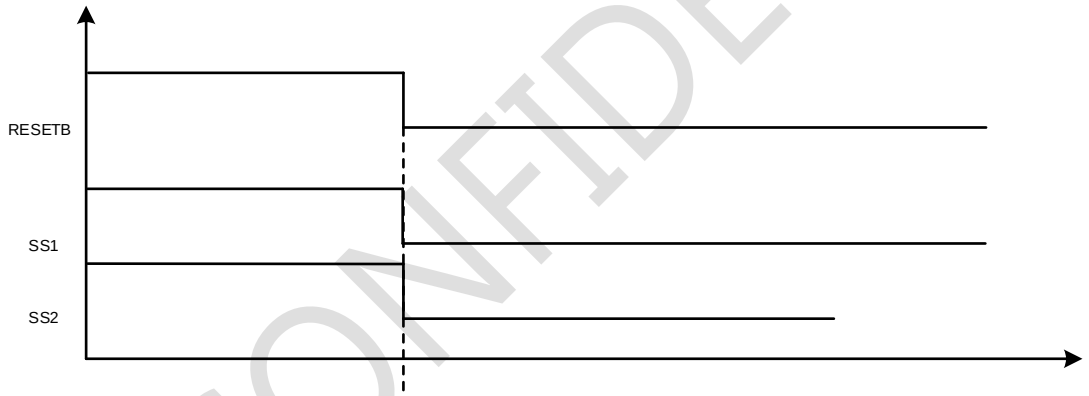

Figure 51. Flow diagram reaction on an error triggered state transition- hard reset

8.4 Reaction on Window Watchdog Output (WWO)

The SCT61490S has an implemented window watchdog failure counter (**WWDSTAT**.**WWDECNT**). The counter increments by two at every invalid window watchdog triggering and decrements by one at every valid window watchdog triggering.
The status of the window watchdog failure counter is written in the so called window watchdog status counter. Any incrementation of the window watchdog status counter is indicated by an interrupt. Any decrementation of thewindow watchdog status counter is not indicated by an interrupt. The content of the window watchdog status counter cannot be less than zero.
The threshold for activating the safe state signals SS1 and SS2 WWO can be changed in INIT, NORMAL and WAKE state. (**WDCFG0**.**WWDETHR**)
The content of the status counter will be compared to the programmed threshold WWO (**RWDCFG0**.**WWDETHR**). If the content of the status counter is equal or higher than WWO, the safe state signals SS1 and SS2 will be activated (low).

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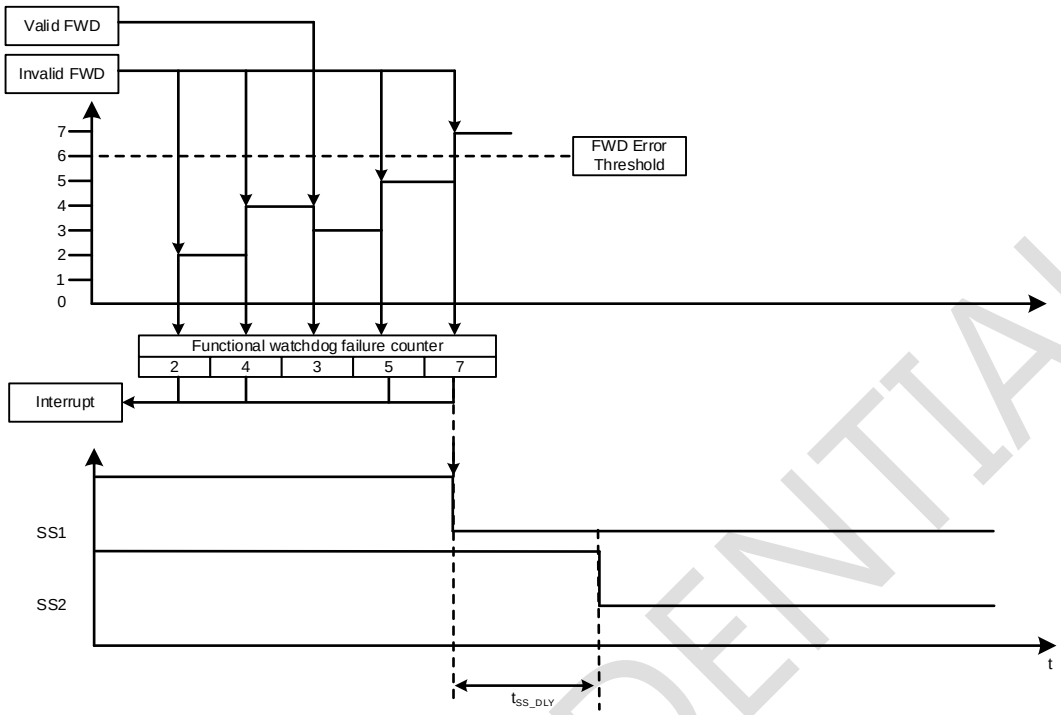

Figure 53. Flow diagram reaction on FWO

8.6 Reaction on Thermal Shutdown (TSD)

The thermal shutdown (TSD) indicates temperature overstress: on the chip: As a consequence all pre and post regulators will be shut down immediately.

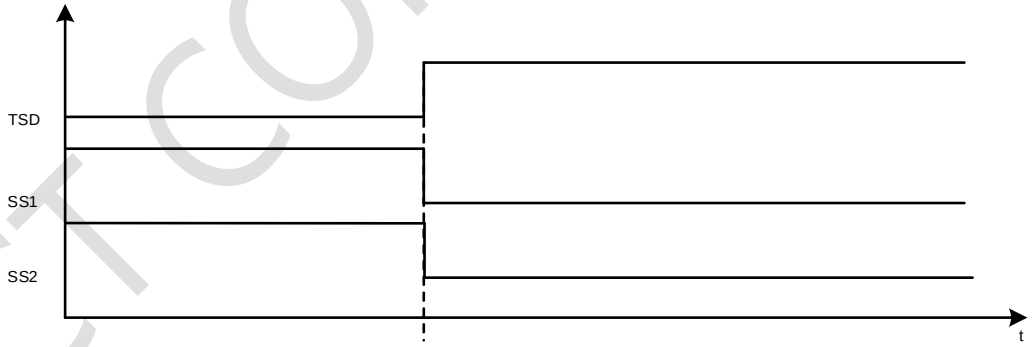

Figure 54. Flow diagram reaction on TSD

9 SPI - Serial Peripheral Interface

9.1 Introduction

Main functions

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10 Interrupt Generation

A dedicated interrupt generation block is implemented which is handling requests from independent sources to generate an interrupt. The different requesters are as follows:

• State machine in case:

– A requested state transition has not been performed successfully, e.g. SLEEP state could not be entered because

– A requested state transition from SLEEP has been performed successfully, i.e. the system has either successfully entered WAKE state. The uC may only send (additional) SPI commands after an interrupt event has been generated by the system. The purpose of the interrupt event is to inform the uC that a state transition has been performed successfully and that the system is capable of performing SPI communication at full SPI speed.

• Watchdog, an interrupt request is generated if the Watchdog is not serviced properly and configured in a way to allow service errors to occur, i.e. an error counter threshold value of more than 2 is configured. In this case an interrupt is generated only if the error counter threshold is not exceeded due to this error.

• Error pin monitoring, an interrupt request is generated if the error pin monitoring block detects an error and is configured in a way to allow occurrence of this error for a certain amount of time (recovery delay action enabled). In this case an interrupt is requested if an error is detected by the error pin monitoring and the recovery delay has not expired.

• Monitoring Block, an interrupt request is generated based on the defined system reaction described in INTERRUPT events

• Overtemperature warnings and over temperature shutdown of communication LDO

• Overcurrent conditions of voltage reference or standby LDO

• SPI block in case an SPI error has occurred

• ABIST operation has been completed

• Double bit error in the protected configuration

An interrupt is generated to inform a connected uC that a non-severe system condition has occurred. This allows the uC to perform proper action based on the source of the interrupt. A single interrupt line exists, which is high on default. All Internal interrupt sources are enabled by default and cannot be disabled.

An interrupt is signaled by pulling the interrupt line low for at least t_{INT} (interrupt min. pulse width) after an internal interrupt condition occurs. The interrupt line will be driven high if all of the **IF** register flag(s) has/have been cleared via SPI operation earliest after t_{INT} has expired but latest after t_{INTTO} has expired.

Special cases:

• If an interrupt is signaled by pulling INTB low and not all interrupt status flags are cleared by the uC within t_{INTTO}, the INT will stay low until t_{INTTO} has expired, but no additional interrupt will be generated. Information about a pending interrupt event can be derived via the INTMISS status flag. This status flag is cleared each time the interrupt line is driven low.

• If an interrupt is signaled by pulling INTB low and an additional bit is set in the **IF** register interrupt flag after the

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Window watchdog trigger pin WDI

The watchdog input pin WDI has an integrated pull-down current I_{WDI_PULL}. The watchdog input WDI can transition to high within the "Closed Window" or during the following "Open Window".

Valid Trigger Signal at WDI

Watchdog input WDI is periodically sampled with a period of t_{WD_SAMPLE}. A valid trigger signal is a falling edge from V_{WDI_H} to V_{WDI_L}. To improve immunity against noise or glitches on the WDI input, at least two high samples followed by two low samples are required for a valid trigger signal, the valid triggering is considered with the second consecutive sampling point measuring low signal. For example, if the first three samples (two high one low) of the trigger pulse at pin WDI are inside the “Closed Window” and only the fourth sample (the second low sample) is taken in the “Open Window” then the watchdog output WWO will indicate “valid WWD triggering”.

Invalid Triggering at WDI

No trigger signal detected during the "Open Window" or a trigger signal detected during the "Closed Window", is considered invalid triggering. Watchdog output WDO indicates “invalid triggering” immediately after no valid trigger

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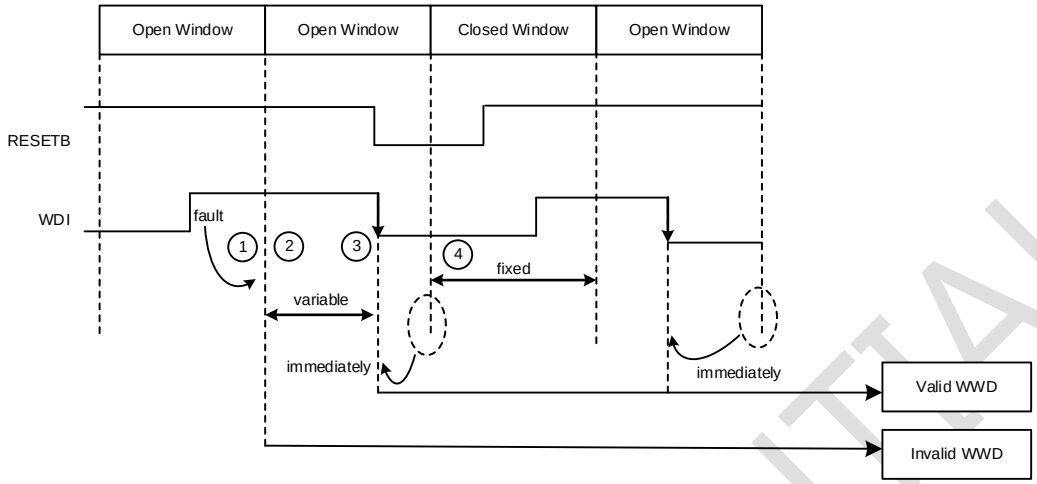

Figure 62. Fault operation: No trigger in Open Window in steady state

1. A missing valid triggering within the “Open Window” leads after the window has ended to an “Invalid WWD triggering”. This event is indicated by an interrupt, the window watchdog failure counter increases by two.
2. Having detected an “Invalid WWD triggering” the watchdog will start a new “Open Window” with duration t_{WD_OW} to give the microcontroller the chance to trigger and synchronize to the watchdog period.
3. A valid triggering terminates the “Open Window”, which makes the duration of the “Open Window” variable and depending on the triggering. This is counted as a “Valid WWD triggering” and a “Closed Window” is started.
The window watchdog failure counter will be decremented by one without an interrupt issued.
Additional informations: In case of multiple “Invalid WWD triggering” within the “Open Windows”, the window watchdog failure counter would be incremented again by two until it reaches the configured threshold. In this case a reset will be issued.
4. The following “Closed Window” lasts for the time t_{WD_CW}. Triggering within this time will be considered as an ”Invalid WWD triggering”.
The behavior of pin RESETB is depending on the value of WWO. In the example above it was assumed, that the invalid triggering will not lead to exceed the threshold WWO.

Incorrect triggering: False trigger in W1D

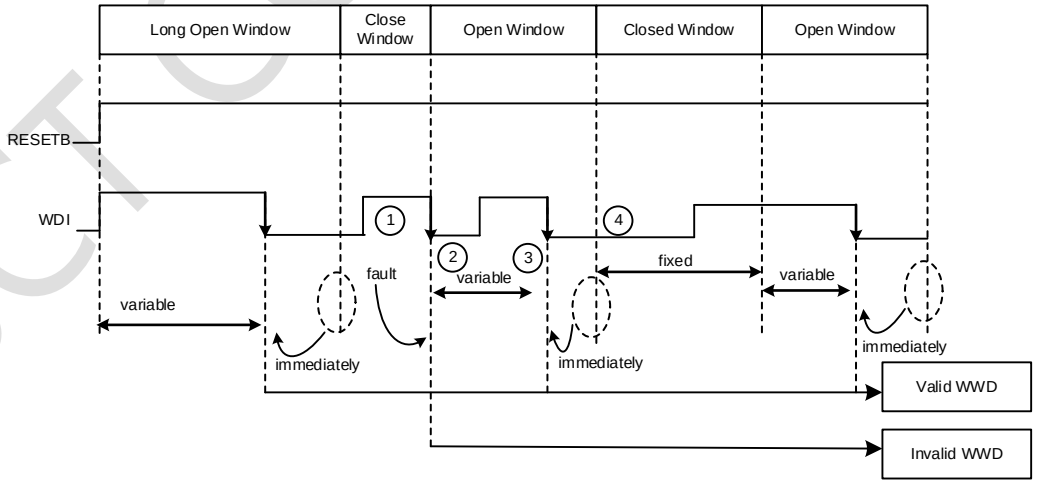

Figure 63. Fault operation: False trigger in Closed Window after initialization

1. A triggering during the “Closed Window” is indicated as “Invalid WWD triggering”. This event is indicated by an

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interrupt and the window watchdog failure counter increases by two.
2. The “Closed Window” will be closed with the “Invalid WWD triggering”. Originally it would last for the time t_{WD_CW}. The false triggering terminates the “Closed Window” and starts an “Open Window” to give the micro processor the opportunity to synchronize to the window watchdog period.
3. Within this “Open Window” a valid triggering is expected. A valid triggering terminates the “Open Window”, which makes the duration of the “Open Window” variable and depending on the triggering. This is counted as a “Valid WWD triggering” and a “Closed Window” is started. The window watchdog failure counter will be decremented by one without an interrupt issued.
4. The following “Closed Window” lasts for the time t_{WD_CW}. Triggering within this time will be considered as an ”Invalid WWD triggering”.
The behavior of pin RESETB is depending on the value of WWO. In the example above it was assumed, that the invalid triggering will not lead to exceed the threshold WWO.

Incorrect triggering: False trigger in close window

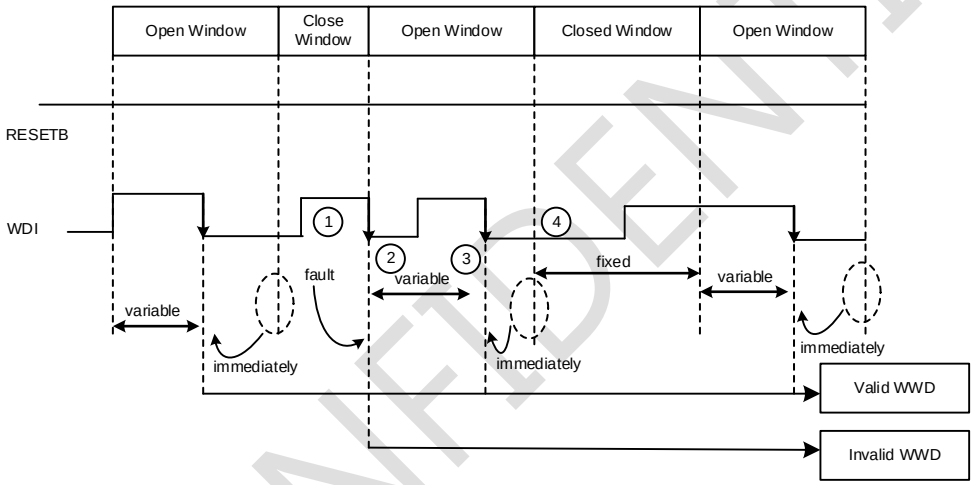

Figure 64. Fault operation: False trigger in Closed Window

1. A triggering during the “Closed Window” is indicated as “Invalid WWD triggering”. This event is indicated by an interrupt and the window watchdog failure counter increases by two.
2. The “Closed Window” will be closed with the “Invalid WWD triggering”. Originally it would last for the time t_{WD_CW}. The false triggering terminates the “Closed Window” and starts an “Open Window” to give the micro processor the opportunity to synchronize to the window watchdog period.
3. Within this “Open Window” a valid triggering is expected. A valid triggering terminates the “Open Window”, which makes the duration of the “Open Window” variable and depending on the triggering. This is counted as a “Valid WWD triggering” and a “Closed Window” is started. The window watchdog failure counter will be decremented by one without an interrupt issued.
4. The following “Closed Window” lasts for the time t_{WD_CW}. Triggering within this time will be considered as an “Invalid WWD triggering”.
The behavior of pin RESETB is depending on the value of WWO. In the example above it was assumed, that the invalid triggering will not lead to exceed the threshold WWO.

11.3 Functional Watchdog

11.3.1 Operation of FWD

Principle of Operation

A functional or question/answer watchdog is integrated in the SCT61490S to monitor the microcontroller. In a steady state a question is generated (taken out of table), in parallel the so called heartbeat counter starts counting from zero. The heartbeat counter counts up, until the heartbeat period has ended. The duration of the heartbeat period

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is set to a default value, but can be adjusted via SPI command. The question consists of 4 bits, the expected answer consists of 4 responses of 8 bits each. The four responses shall be sent before the heartbeat period has ended. The last response shall be written to the synchronized response register to reset the heartbeat counter.

Initialization

The functional watchdog is off per default when the device is powered up for the first time. It can be enabled by SPI writing to **WDCFG0**.**FWDEN**.

Configuration

The functional watchdog can be configured in INIT, NORMAL and WAKE state. “Configured” means:

• Modify the length of the heartbeat period by SPI command, depending on the needs of the application. (combination of cycle time **WDCYC** and number of cycles for heartbeat **WDHBTP**)

• The threshold for the functional watchdog failure counter overflow can defined by SPI The heartbeat period is based on the cycle time t_{CYCLE}.

Normal Operation

The question is taken out of the below table, the correct responses are listed in the same row. The sequence of responses must be kept and can be derived from the response counter **FWDSTAT0**.**FWDRSPC** before sending the response.

The response to the actual question defined in the table shall be composed by four subsequent response bytes. A correct response to the given question in **FWDSTAT0**.**FWDQUEST** register shall be done in the following way.

• The first three responses shall be written into **FWDRSP**

• The last response should be written into **FWDRSPSYNC** to reset the heartbeat timer

All four responses must be written before the heartbeat period expires.

If the complete response (32 bits) is correct and if the last response byte was sent with synchronized respond, the heartbeat counter will be reset and set to zero. If the complete answer (all four responses - 32 bits) is correct, it is regarded as “Valid FWD triggering”, the functional watchdog error counter FWO is decremented by 1. If the last response was sent with synchronized response, the heartbeat counter will be reset, but if the answer is wrong, this is regarded as “Invalid FWD triggering” and the functional watchdog error counter FWO is incremented by 2.

An overflow of the functional watchdog error counter FWO will trigger a “Move to INIT” event, reset the heartbeat counter and set the functional watchdog error counter FWO to zero.

Table 10 Functional watchdog response definition

QUESTION	RESP3	RESP2	RESP1	RESP0
0	FF	0F	F0	00
1	B0	40	BF	4F
2	E9	19	E6	16
3	A6	56	A9	59
4	75	85	7A	8A
5	3A	CA	35	C5
6	63	93	6C	9C
7	2C	DC	23	D3
8	D2	22	DD	2D
9	9D	6D	92	62
A	C4	34	CB	3B
B	8B	7B	84	74
C	58	A8	57	A7
D	17	E7	18	E8
E	4E	BE	41	B1
F	01	F1	0E	FE

Functional watchdog output FWO

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the functional watchdog FWO output is either “Valid FWD triggering” or “Invalid FWD Triggering”.

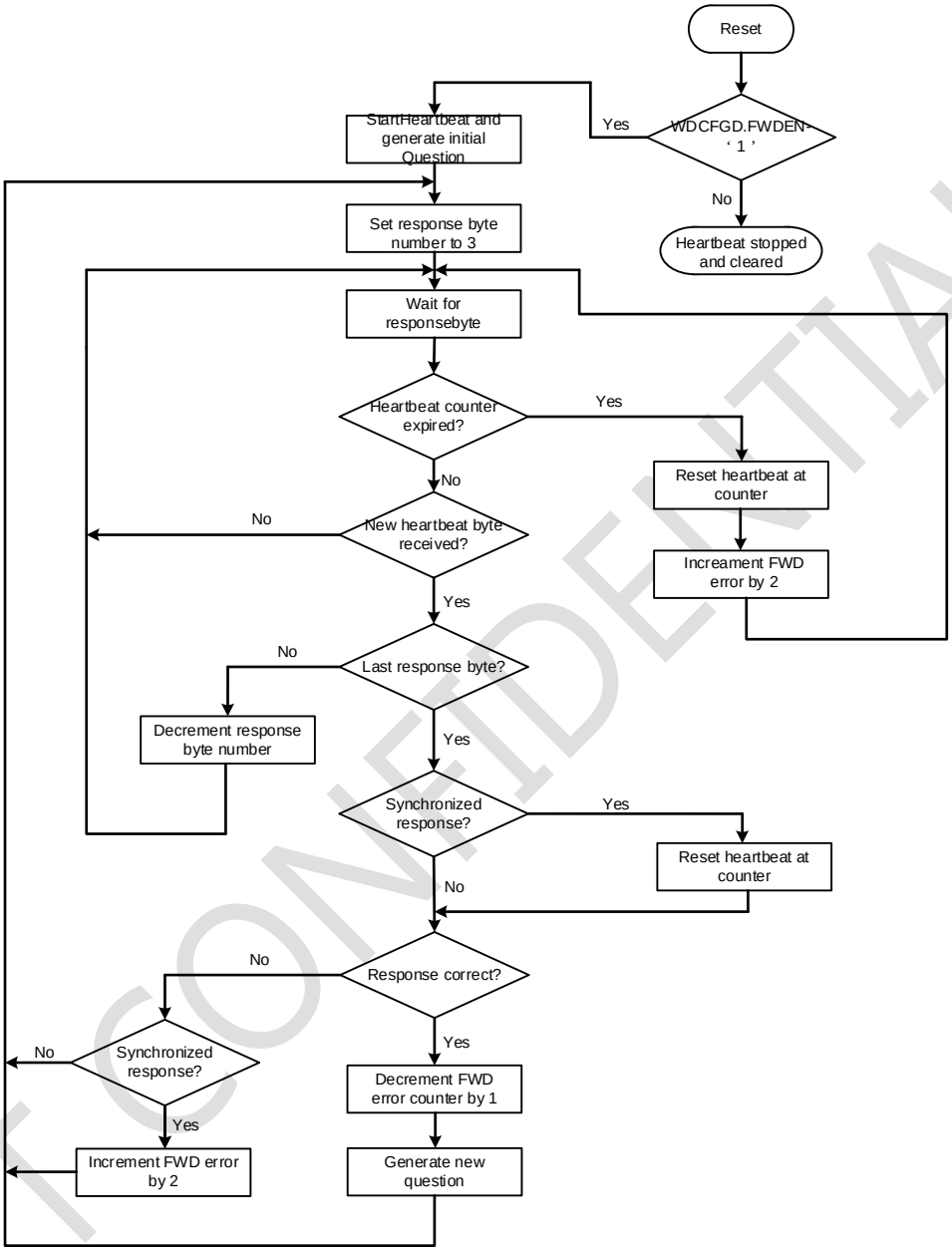

Figure 65. Functional watchdog flowchart diagram

11.3.2 Timing Diagrams

Correct triggering

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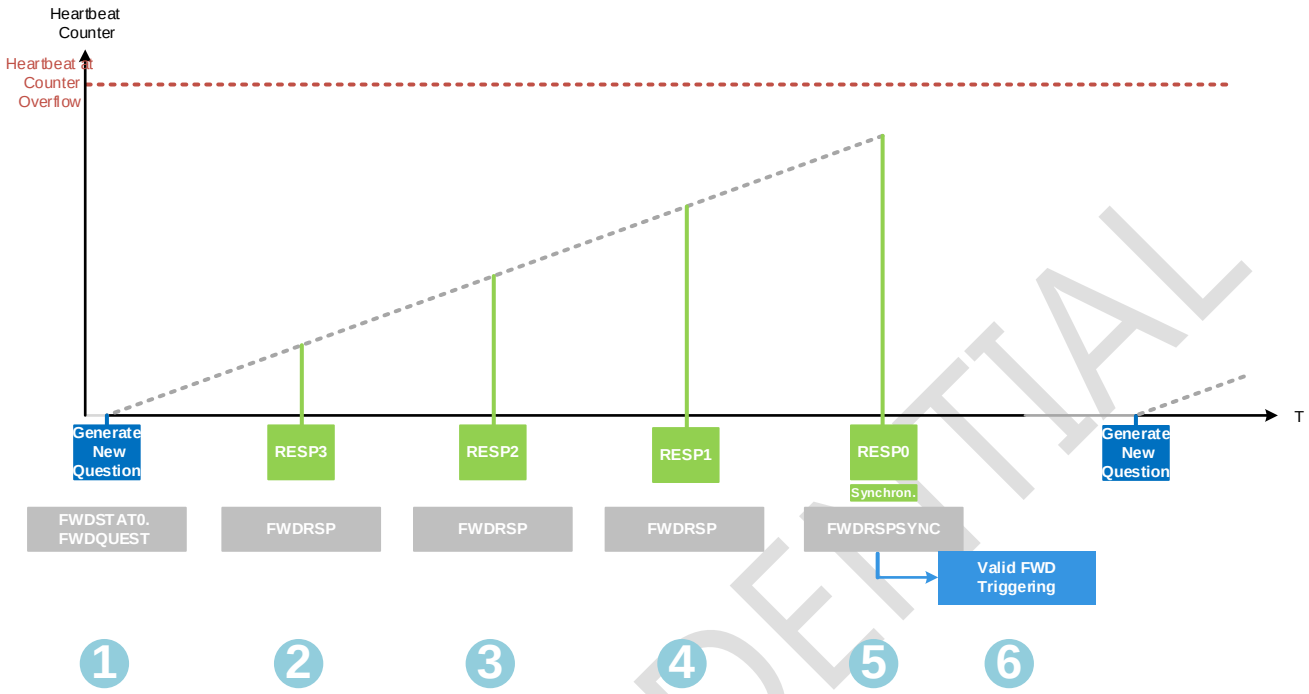

Figure 66. Normal operation: Correct triggering

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a “Valid FWD triggering” has happened before).
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. A correct response is received (RESP1)
5. A correct synchronized response is received (RESP0). All responses are correct, the sequence of responses is correct and the last synchronized response was received before the heartbeat counter overflowed. The heartbeat counter will be reset (set to zero). This is regarded as “Valid FWD triggering”, the functional watchdog error counter FWO is decremented by 1 (if the functional watchdog error counter value is higher than zero).
6. A new question is generated, in parallel the heartbeat counter starts counting up

Incorrect triggering: Synchronization is missing

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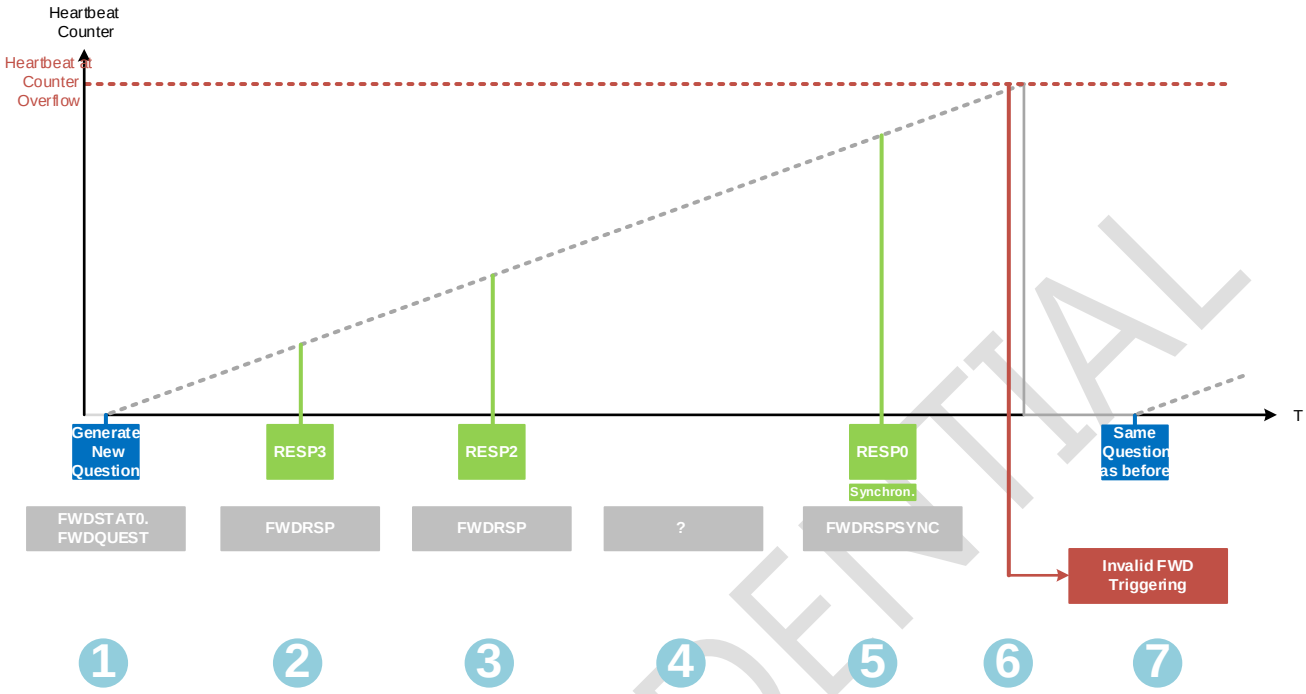

Figure 69. Fault operation: Answer is not complete

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a “Valid FWD triggering” has happened before).
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. A response is missing (RESP1)
5. A correct response is received (RESP0). So the last response is not the last response but the second last due to the missing response (in this example RESP1). The functional watchdog will wait for all four responses to be written, while the heartbeat counter keeps on counting. There is no fixed time for all four responses, but they must be sent in correct order before the heartbeat counter expires.
6. The complete answer is not correct due to missing response RESP1. Although the last response is synchronized, the heartbeat counter will not be reset and continue counting up until an overflow occurs. This is regarded as “Invalid FWD triggering”. The functional watchdog error counter FWO is incremented by 2. The heartbeat counter is reset.
7. No new question is generated and the heartbeat counter starts counting up.

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12 Typical Application

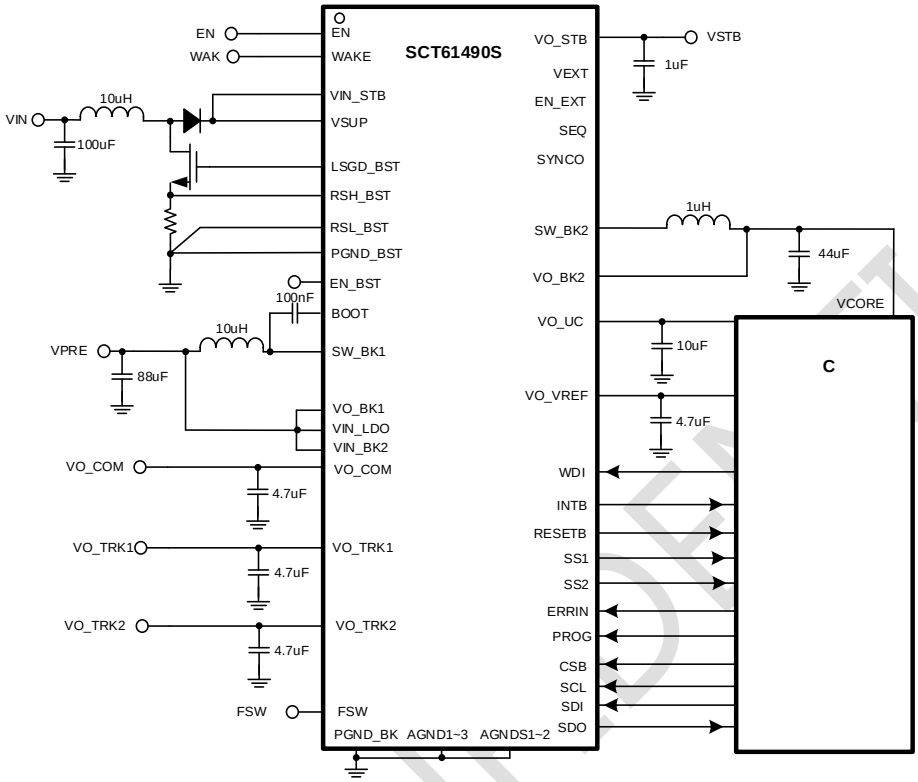

Figure 70. Application Schematics, 3V to 40V Input

Design Parameters	Example Value
Input Voltage	12V Nominal 3V to 40V
Output Voltage	VO_BK1: 5.8V VO_BK2: 1.2V VO_UC: 5V VO_STB: 5V VO_COM: 5V VO_VREF: 5V VO_TRK1/2: 5V
Maximum Output Current	VO_BK1: 4A VO_BK2: 5A VO_UC: 800mA VO_STB: 20mA VO_COM: 600mA VO_VREF: 200mA VO_TRK1/2: 200mA
Switching Frequency	400kHz/2.2MHz (selectable)

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The SCT61490S is featured with minimized external components and any feedback divider or configuration resistor could be saved. For typical application, the recommended inductance and capacitance for each power rail are listed in Table 11. Higher inductance and capacitance for lower output ripple are also acceptable.

Table 11. Recommended BOM for Typical Application

Power Rail	Switching Frequency	Inductor	Output Capacitor
VO_BK1: 5.8V	400kHz	10~22uH	10~47uF
VO_BK1: 5.8V	2.2MHz	4.7~10uH	68~100uF
VO_BK2: 1.2V	2.2MHz	1uH	44uF
VO_UC: 5V	-	-	2.2~47uF

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Application Waveforms (continued)

V_{IN} = 12V, V_{BK1} = 5.8V, V_{BK2} = 1.2V, V_{UC} = 5V, V_{STB} = 5V, V_{COM} = 5V, V_{VREF} = 5V, V_{TRK12} = 5V, L1 = 10uH, L2 = 1uH, T_A = 25°C, unless otherwise noted.

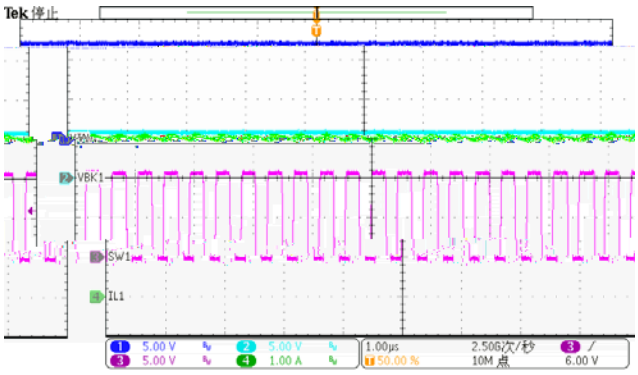

Figure 77. Buck1 Steady State, Load=4A

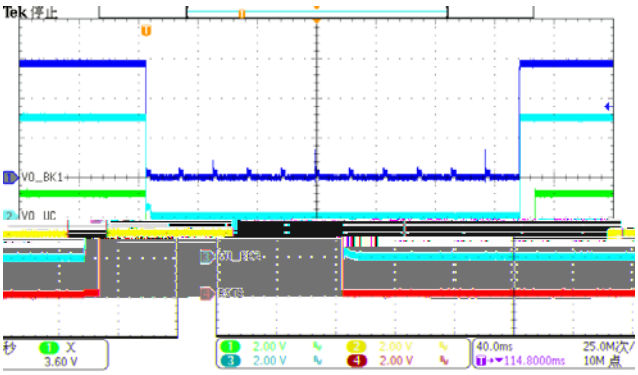

Figure 78. Buck1 Short-circuit and Recovery

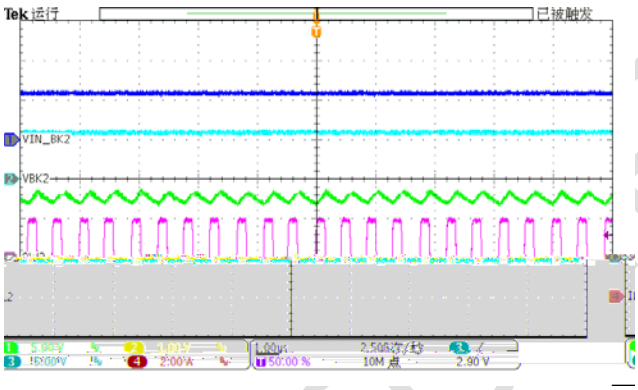

Figure 79. Buck2 Steady State, Load=5A

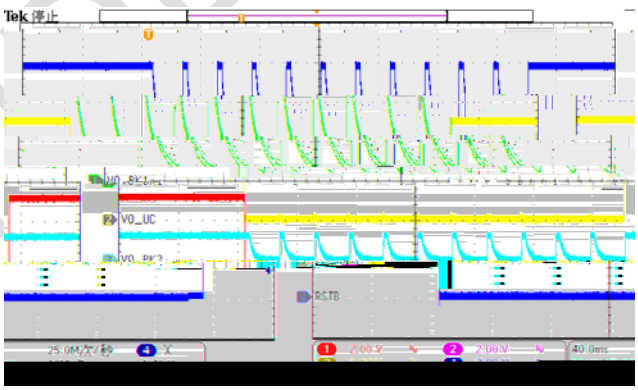

Figure 80. VO_UC Short-circuit and Recovery

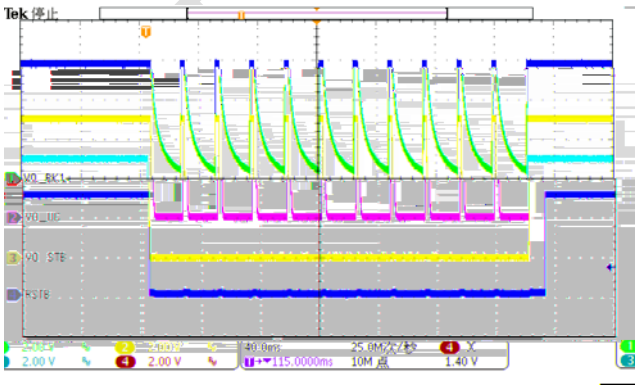

Figure 81. VO_ STB Short-circuit and Recovery

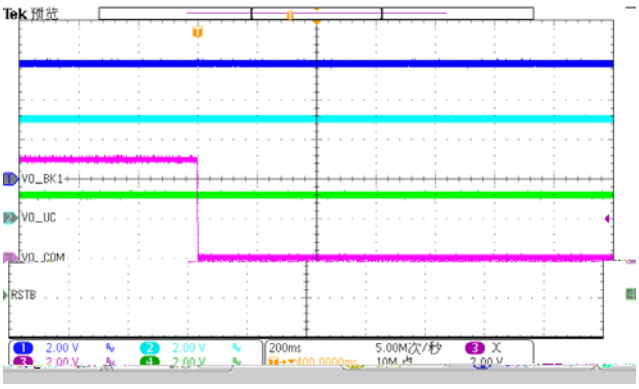

Figure 82. VO_COM Short-circuit

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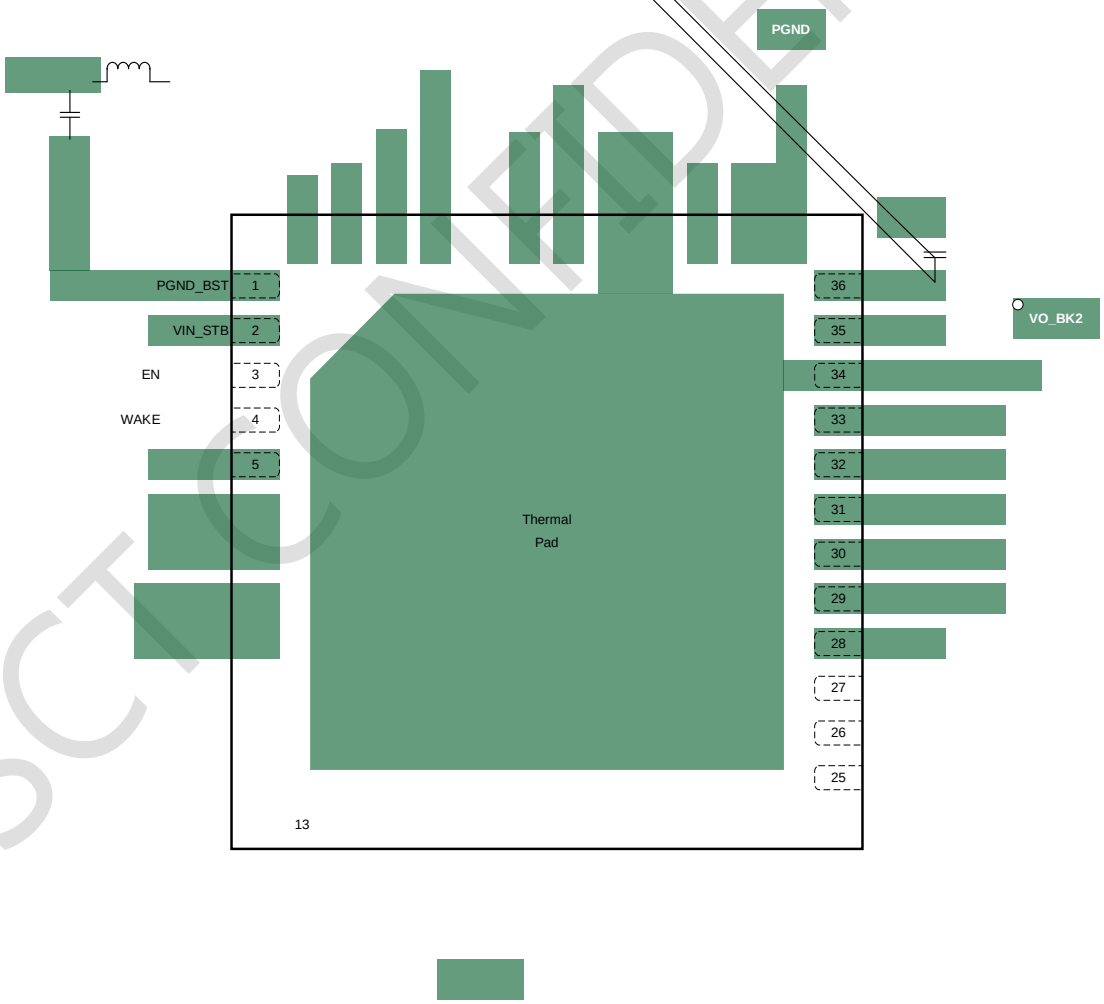
12.2 Layout Guideline

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The rule of thumb is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over-heat area.
2. Place a low ESR ceramic capacitor as close to VIN, VIN_BK2 and VIN_LDO pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.
5. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. Connect AGND to PGND plane at a single point.



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13 Register Decription

13.1 Register Type Abbreviations

Abbreviations	Description
R0	Reset type 0. Registers that are being reset only in case of a POR.
R1	Reset type 1. Registers that are being reset only in case of STANDBY and a POR.
R2	Reset type 2. Registers that are being reset only in case of FAILSAFE, STANDBY and a POR.
R3	Reset type 3. Registers that are being reset in case of “Move to INIT” event, FAILSAFE, STANDBY and a POR.
R	Bits that are readable only (read)
RW	Bits that are readable and writable (read-write)
RWP	Bits that are readable and writable but protected by register PROTCFG (read-write-protected)
RW1C	Bits that are readable and to clear the bit you have to write a 1 to it. (read-write-1-to-clear). Flag-bits are updated based on the occurred condition.
RWHC	Bits that are readable and writable after writing the operation is triggered, once this is done successfully the bit is cleared by hardware. (read-write-hardware-cleared)
RWHU	Bits that are readable and writable, after the operation the bit is updated by hardware. (read-write- hardware-updated)

13.2 Register Mapping

ADDRESS	REGISTER	DEFAULT VALUE	RESET TYPE
0x00	DEVCFG0	08h	R2
0x01	DEVCFG1	06h	R0
0x02	DEVCFG2	00h	R2
0x03	PROTCFG	00h	R2
0x04	SYSPCFG0	01h	R1
0x05	SYSPCFG1	08h	R2
0x06	WDCFG0	9Bh	R2
0x07	WDCFG1	09h	R2
0x08	FWDCFG	0Bh	R2

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[0]	ESYNEN	RW	Synchronization output for external switchmode regulator enable	0 = Disabled 1 = Enabled

PROTCFG [7:0]				
ADDRESS: 0x03				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	CTHR	RW	Protection key Protection key register to request write access to protected registers. Unlock: write 32-bit sequence of 4 consecutive bytes (1: 0xAB 2:0xEF 3:0x56 4:0x12) to unlock access to protected registers. Lock: write 32-bit sequence of 4 consecutive bytes (1: 0xDF 2:0x34 3:0xBE 4:0xCA) to lock access to protected registers. All configured values are applied to SSC and WD module after the lock.	ABh = Key 1 to unlock protected registers. EFh = Key 2 to unlock protected registers. 56h = Key 3 to unlock protected registers. 12h = Key 4 to unlock protected registers. DFh = Key 1 to lock protected registers. 34h = Key 2 to lock protected registers. BEh = Key 3 to lock protected registers. CAh = Key 4 to lock protected registers.

SYSPCFG0 [7:0]				
ADDRESS: 0x04				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:1]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[0]	STBYEN	RW	Request standby regulator VO_STB enable	0 = Disabled 1 = Enabled

SYSPCFG1 [7:0]				
ADDRESS: 0x05				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	SS2DEL	RWP	Request safe state 2 delay Applied for transitions from NORMAL to INIT, WAKE and SLEEP state.	000 = no delay; 001 = 10ms; 010 = 50ms; 011 = 100ms; 100 = 250ms; 101 = 1250ms; 110 = 2500ms
[4]	ERRSLPEN	RWP	Request ERR pin monitor functionality enable while the system is in SLEEP	0 = ERRIN pin monitor is disabled in SLEEP 1 = ERRIN pin monitor can be active in SLEEP depending on ERREN bit value.
[3]	ERREN	RWP	Request ERRIN pin monitor enable	0 = Step-down converter runs on low frequency range 1 = Step-down converter runs on high frequency range
[2]	ERRRECEN	RWP	Request ERRIN pin monitor recovery enable	0 = Disabled 1 = Enabled
[1:0]	ERRREC	RWP	Request ERRIN pin monitor recovery time	00 = 1ms; 01 = 2.5ms; 10 = 5ms; 11 = 10ms

WDCFG0 [7:0]

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ADDRESS: 0x06				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	WWDETHR	RWP	Request window watchdog error threshold WWD error threshold to generate reset and enter into INIT state.	WWD error thrshold = WWDETHR[3:0] * 1 times
[3]	WWDE	RWP	Request window watchdog enable	0 = Disabled 1 = Enabled
[2]	FWDEN	RWP	Request functional watchdog enable	0 = Disabled 1 = Enabled
[1]	WWDTSEL	RWP	Request window watchdog trigger selection This is ignored when window watchdog is disabled.	0 = External WDI input used as a WWD trigger 1 = WWD is triggered by SPI write to WWDSCMD register
[0]	WDCYC	RWP	Request watchdog cycle time	0 = 0.1 ms tick period 1 = 1 ms tick period

WDCFG1 [7:0]				
ADDRESS: 0x07				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[6]	WDCYCDIV	RWP	Request enable of additional divider by 10 for watchdog cycle time (WDCYC) configuration, Data bits are sent inverted to SPI upon read access.	0 = Disabled 1 = Enabled, additional divider by 10 for watchdog cycle time (WDCYC) configuration is enabled
[5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4]	WDSLPEN	RWP	Request watchdog functionality enable while the device is in SLEEP	0 = Disabled 1 = Enabled, the WD will work based on individual configuration (WWDEN & FWDEN) settings while the system is in SLEEP mode
[3:0]	FWDETHR	RWP	Request functional watchdog error threshold FWD error threshold to generate reset and enter into INIT state.	FWD error thrshold = FWDETHR[3:0] * 1 times

FWDCFG [7:0]				
ADDRESS: 0x08				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4:0]	WDHBTP	RWP	Request functional watchdog heartbeat timer period Defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC).	Heartbeat timer period = (WDHBTP[4:0]+1)* 50 WD cycles

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			Current configuration of ERR pin monitor enable.	1 = Enabled
[2]	ERRRECEN	R	ERRIN pin monitor recovery enable status Current configuration of ERR pin monitor recovery enable.	0 = Disabled 1 = Enabled
[1:0]	ERRREC	R	Request watchdog cycle time	00 = 1ms; 01 = 2.5ms; 10 = 5ms; 11 = 10ms

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[3:0]	FWDETHR	R	Request functional watchdog error threshold FWD error threshold to generate reset and enter into INIT state.	FWD error thrshold = FWDETHR[3:0] * 1 times

RFWDCFG [7:0]				
ADDRESS: 0x0F				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4:0]	WDHBTP	R	Request functional watchdog heartbeat timer period Defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC).	Heartbeat timer period = (WDHBTP[4:0]+1)* 50 WD cycles

RWWDCFG0 [7:0]				
ADDRESS: 0x10				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4:0]	CW	R	Request window watchdog closed window time Defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC).	WWD close window= (CW[4:0]+1)* 50 WD cycles

RWWDCFG1 [7:0]				
ADDRESS: 0x11				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4:0]	OW	RWP		

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BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7:0]	TIMVALM	RW	Wake timer value middle bits Bits (15:8) of wake time defined as a multiple of wake timer cycles (DEVCFG0.WKTIMCYC).	

WKTIMCFG2 [7:0]				
ADDRESS: 0x14				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	TIMVALH	RW	Wake timer value higher bits Bits (23:16) of wake time defined as a multiple of wake timer cycles (DEVCFG0.WKTIMCYC).	

DEVCTRL [7:0]				
ADDRESS: 0x15				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2EN	RW	Request LDO tracker2 enable	0 = TRK2 will be disabled after valid request 1 = TRK2 will be enabled after valid request
[6]	TRK1EN	RW	Request LDO tracker1 enable	0 = TRK1 will be disabled after valid request 1 = TRK1 will be enabled after valid request
[5]	COMEN	RW	Request communication LDO_COM enable	0 = LDO_COM will be disabled after valid request 1 = LDO_COM will be enabled after valid request
[4]	BK2_EN	RW	Request LV Buck 2 enable	0 = LV Buck 2 will be disabled after valid request 1 = LV Buck 2 will be enabled after valid request
[3]	VREFEN	RW	Request voltage reference LDO_VRF enable	0 = LDO_VRF will be disabled after valid request 1 = LDO_VRF will be enabled after valid request
[2:0]	STATEREQ	RWHC	Request for device state transition Cleared to 000 by the HW after the request is processed. After writing a new state value a user should not change the value before it's cleared by HW.	000 = NONE; 001 = INIT; 010 = NORMAL; 011 = SLEEP; 100 = STANDBY; 101 = WAKE; 110 = RESERVED; 111 = RESERVED

DEVCTRLN [7:0]				
ADDRESS: 0x16				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2EN	RW	Request LDO tracker2 enable	1 = TRK2 will be disabled after valid request

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SYSFAIL [7:0]				
ADDRESS: 0x1A				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	INITF	RW1C	INIT failure flag INIT failure due to the third INIT failure in row. i.e. The device restarts INIT phase from FAILSAFE.	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags
[6]	ABISTERR	RW1C	ABIST operation interrupted flag ABIST interrupted by any fault/event which is not part of ABIST.	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags
[5:4]	RSV	R	Reserved	
[3]	RSTB_MON_ERR	RW1C	RESETB monitor failure flag	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags
[2]	VMONF	RW1C	Voltage monitor failure flag Voltage monitor failure occured which lead to FAILSAFE.	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags, read MONSF0, MONSF1 and MONSF3 for details
[1]	OTF	RW1C	Over temperature failure flag	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags, read OTFAIL for details
[0]	VOLTSELER R	RW1C	Double Bit error on voltage selection flag Device entered FAILSAFE state due to internal voltage selection failure.	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags

INITERR [7:0]
ADDRESS: 0x1B

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				1 = Fault occurred, write 1 to clear the flags
[2]	VMONF	RW1C	Voltage monitor failure flag Voltage monitor failure occured which lead to FAILSAFE.	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags, read MONSF2 for details
[1]	CRG_ERR	RW1C	clock monitor or reset monitor failure flag.	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags
[0]	RSV	RW1C	Reserved	

IF [7:0]				
ADDRESS: 0x1C				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	INTMISS	R	Interr.959 req 88.56 547.56 68.7ADDRESSIND 23 >>BDC145	

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			Transition to low power failed either due to the LDO_UC current monitor, WAK high level or a rising edge on EN PIN during TRDEL time.	1 = Event detected, write 1 to clear the flag
[3]	ERRMISS	RW1C	MCU error miss status flag Set only when SYSPCFG1.ERRRECEN='1'	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	FWDE	RW1C	Functional watchdog error interrupt flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	WWDE	RW1C	Window watchdog error interrupt flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	CFGE	RW1C	Protected configuration double bit error flag Double bit error occurred on protected configuration register. Status registers shall be read in order to determine which configuration has changed.	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

WKSF [7:0]				
ADDRESS: 0x1E				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	WAKST	R	WAKE input status	0 = Voltage at pin WAKE is in low level signal range 1 = Voltage at pin WAKE is in high level signal range
[6]	ENST	R	EN input status	0 = Voltage at pin EN is in low level signal range 1 = Voltage at pin EN is in high level signal range
[5]	RSV	R	Reserved	
[4]	WKSPI	RW1C	Wakeup from SLEEP by SPI flag (GoToWAKE)	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	WKTIM	RW1C	Wake timer wakeup flag Bit will also be set if STANDBY state left because of wake timer expired.	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	CMON	RW1C	LDO_UC current monitor threshold wakeup flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	EN	RW1C	EN signal wakeup flag Bit will also be set if FAILSAFE or STANDBY state left because of EN.	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	WAKE	RW1C	WAKE signal wakeup flag Bit will also be set if FAILSAFE or STANDBY state left because of WAK.	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

SPISF [7:0]

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				1 = Event detected, write 1 to clear the flag
[6]	TRK1OV	RW1C	Tracker1 over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[5]	VREFOV	RW1C	Voltage reference over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[4]	COMOV	RW1C	Communication LDO over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	VEXTOV	RW1C	External voltage over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	STBYOV	RW1C	Standby LDO over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	UCOV	RW1C	uC LDO over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	BK1OV	RW1C	Pre-Buck1 voltage over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

MONSF2 [7:0]				
ADDRESS: 0x22				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2UV	RW1C	Tracker2 under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[6]	TRK1UV	RW1C	Tracker1 under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[5]	VREFUV	RW1C	Voltage reference under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[4]	COMUV	RW1C	Communication LDO under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	VEXTUV	RW1C	External voltage under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	STBYUV	RW1C	Standby LDO under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	UCUV	RW1C	uC LDO under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	BK1UV	RW1C	Pre-Buck1 voltage under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

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MONSF3 [7:0]				
ADDRESS: 0x23				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	BIASHI	RW1C	Bias current too high flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[6]	BIASLOW	RW1C	Bias current too low flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[5]	BG12OV	RW1C	Bandgap comparator over voltage condition flag (VBG1 VBG2 + 4%)	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[4]	BG12UV	RW1C	Bandgap comparator under voltage condition flag (VBG1 VBG2 - 4%)	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	BK2SG	RW1C	LV Buck2 short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	BK2OV	RW1C	LV Buck2 over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	BK2UV	RW1C	LV Buck2 under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	VBATOV	RW1C	Supply voltage VSUP over voltage flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

OTFAIL [7:0]				
ADDRESS: 0x24				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	MON	RW1C	Monitoring over temperature flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[6:5]	RSV	R	Reserved	
[4]	COM	RW1C	Communication LDO over temperature flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	BK2	RW1C	LV Buck2 over temperature flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	RSV	R	Reserved	
[1]	UC	RW1C	uC LDO over temperature flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	BK1	RW1C	Pre-Buck1 over temperature flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

OTWRNSF [7:0]

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ADDRESS: 0x25				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RSV	R	Reserved	
[5]	VREF	RW1C	Voltage reference over load flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[4]	COM	RW1C	Communication LDO over temperature warning flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	BK2	RW1C	LV Buck2 over temperature warning flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	STDBY	RW1C	Standby LDO over load flag (over current for more than 1ms)	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	UC	RW1C	uC LDO over temperature warning flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	PREG	RW1C	Pre-regulator over temperature warning flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

VMONSTAT [7:0]				
ADDRESS: 0x26				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2ST	R	Tracker2 voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK
[6]	TRK1ST	R	Tracker1 voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK
[5]	VREFST	R	Voltage reference voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK
[4]	COMST	R	Communication LDO voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK
[3]	VEXTST	R	External voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK
[2]	STBYST	R	Standby LDO voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK
[1]	RSV	R	Reserved	
[0]	BK1ST	R	Pre-regulator voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK

DEVSTAT [7:0]				
ADDRESS: 0x27				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**

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[7]	TRK2EN	R	Tracker2 voltage enable status	0 = Voltage is disabled 1 = Voltage is enabled
[6]	TRK1EN	R	Tracker1 voltage enable status	0 = Voltage is disabled 1 = Voltage is enabled
[5]	COMEN	R	Communication LDO enable status	0 = Voltage is disabled 1 = Voltage is enabled
[4]	STBYEN	R	Standby LDO enable status	0 = Voltage is disabled 1 = Voltage is enabled
[3]	VREFEN	R	Reference voltage enable status	0 = Voltage is disabled 1 = Voltage is enabled
[2:0]	STATE	R	Device state	000 = NONE; 001 = INIT; 010 = NORMAL; 011 = SLEEP; 100 = STANDBY; 101 = WAKE; 110 = RESERVED; 111 = RESERVED

PROSTAT [7:0]				
ADDRESS: 0x28				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	KEY4OK	R	Key4 ok status Information about validity of the 4th received protection key byte	0 = Key not valid 1 = Key valid

[6]

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ABIST_SELECT0 [7:0]				
ADDRESS: 0x2E				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2OV	RWHU	Select TRK2 OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[6]	TRK1OV	RWHU	Select TRK1 OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[5]	VREFOV	RWHU	Select VREF OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[4]	COMOV	RWHU	Select COM OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[3]	VEXTOV	RWHU	Select External voltage OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[2]	STBYOV	RWHU	Select Standby LDO OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[1]	UCOV	RWHU	Select uC LDO OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[0]	PREGOV	RWHU	Select Pre-regulator OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

ABIST_SELECT1 [7:0]				
ADDRESS: 0x2F				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2UV	RWHU	Select TRK2 UV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

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				comparator, bit will be set in case of ABIST fail for this comparator
[4]	BG12UV	RWHU	Bandgap comparator under voltage condition flag	

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BCK_FRE_SPREAD [7:0]				
ADDRESS: 0x32				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	FRE_SP_THR	RW	Spread spectrum Select the percentage of frequency spread(+/-). The mean frequency is reduced by the percentage as well keeping the maximum frequency at the nominal frequency selected by FRE.	00h = No change; 2Bh = 1% 55h = 2% 80h = 3% AAh = 4% D5h = 5% FFh = 6% C4h = 10% others = No change

BK1_CTRL [7:0]				
ADDRESS: 0x33				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	BUSY	R	DATA_VALID parameter update ready status	0 = update done 1 = update ongoing
[6]	BCK_FREQ_ SEL	RW	Enable buck update Update Command to load new parameter for stepdown regulator (after configuration write 1 to update and write 0 after BUSY flag is cleared to proceed operation)	0 = No action 1 = Load new parameters
[5:1]	RSV	R	Reserved	
[0]	BK2DVS_UNLOCK	RW	BK2DVS and BK2DVSN unlock bit	0 = lock 1 = unlock

BK2DVS [7:0]				
ADDRESS: 0x34				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	BK2_OV_SEL	RW	Interal Post Buck OV monitor threshold Register	00 = OV rising threshold is VSET*106%, falling thrshold is VSET*105%; 01 = OV rising threshold is VSET*104%, falling thrshold is VSET*103%; 10 = OV rising threshold is VSET*108%, falling thrshold is VSET*107%; 11 = OV rising threshold is VSET*110%, falling thrshold is VSET*109%.
[6:0]	BK2DVS	RW	Internal Post Buck Output Voltage Program Request Register	VOUT2=LVDVS[6:0]*10mV+600mV, 600mV~1870mV (720mV~1800mV) 0000000 = 0.60V; 0000001 = 0.61V; 0000010 = 0.62V; 0000011 = 0.63V;

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				… 1111100 = 1.84V; 1111101 = 1.85V;1111110 = 1.86V; 1111111 = 1.87V.

BK2DVSN [7:0] 111184.4044 04D 6 56 0D9 12.84 re 3783.52 0.9401783791.150.28.96 -0 0 904 213.6 30.77.64

ADDRESS: 0

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[1]	VREF_OPEN	RW1C	Vref LDO cap open status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	RSV	R	Reserved	N/A

SYS_STAT2 [7:0]				
ADDRESS: 0x3C				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	PROG	RW	MCU programming support enable(OR combination with PROG pin)	0 = Disabled via SPI(unless enabled by PROG pin high) 1 = Enabled via SPI(independent of PROG pin)
[6]	MPSIN	R	MCU programming support enable(OR combination with PROG bitfield)	0 = Disabled via pin PROG(unless enabled by PROG bitfield being set) 1 = Enabled via pin PROG(independent of PROG bitfield)
[5:0]	CYCMON	R	Watchdog cycle timer monitor	0D 0 wd cycles passed 1D 1 wd cycles passed 2D 2 wd cycles passed ... 50D 50 wd cycles passed 51D not used ... 63D not used

CHIP_CODE [7:0]				
ADDRESS: 0x3D				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	CHIP_CODE	RW	Chip Suffix Code	Chip Suffix Code, refer to Rev Note.

GTM [7:0]				
ADDRESS: 0x3F				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:2]	RSV	R	Reserved	N/A
[1]	NTM	R	Test mode inveted status	0 = Device is in test mode 1 = Device is in normal mode
[0]	TM	R	Test mode status	0 = Device is in normal mode 1 = Device is in test mode

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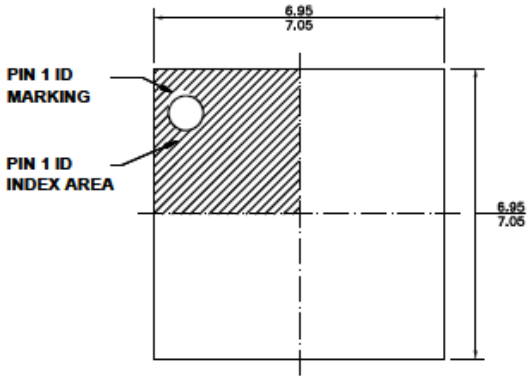
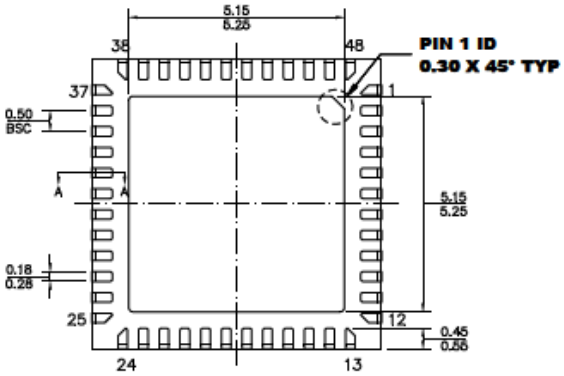
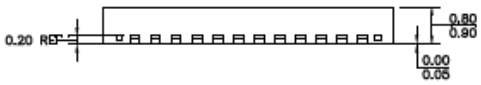
PACKAGE INFORMATION



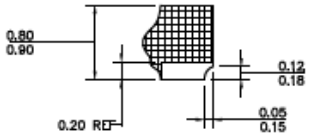
TOP VIEW



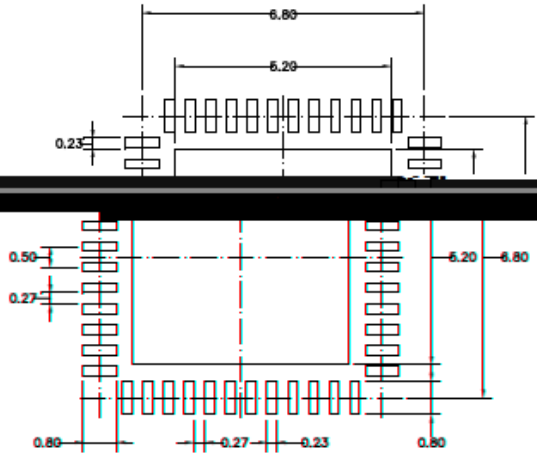
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD-SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) DRAWING CONFIRMS TO JEDEC MO-220.
6) DRAWING IS NOT TO SCALE.

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