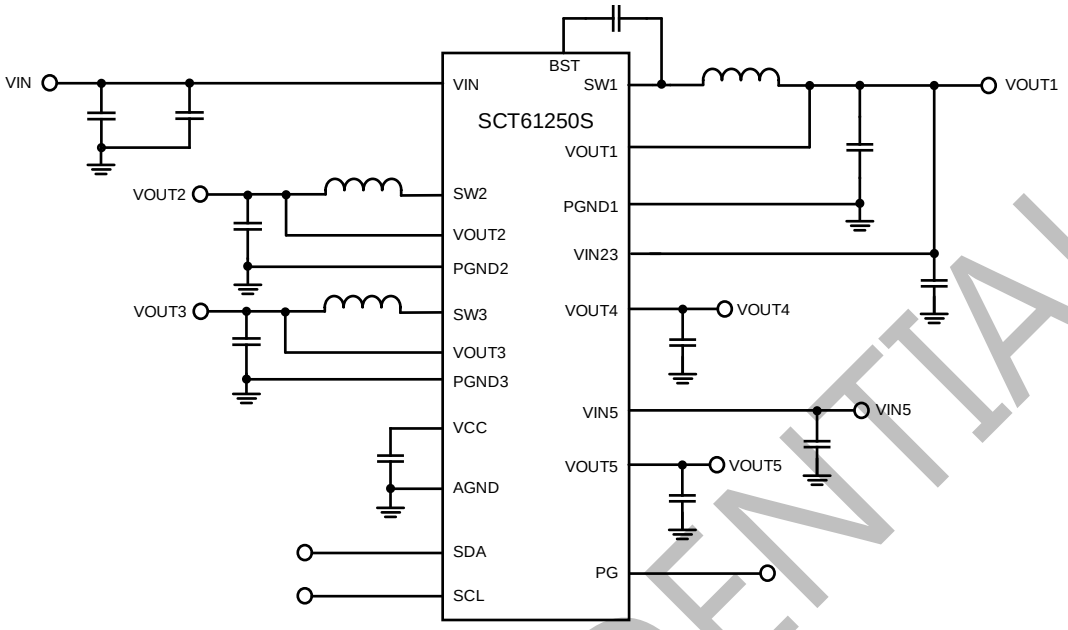
19V Vin Five-Channel Power Management IC for Safety Applications

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -

TYPICAL APPLICATION



REVISION HISTORY

Revision 1.0: Release to market.

Revision 1.1: Updated package description, added application information and fixed few typos.

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT61250S-xxxxQHBR	Tape & Reel	5000	1250S	20	QFN3X3-20L	1

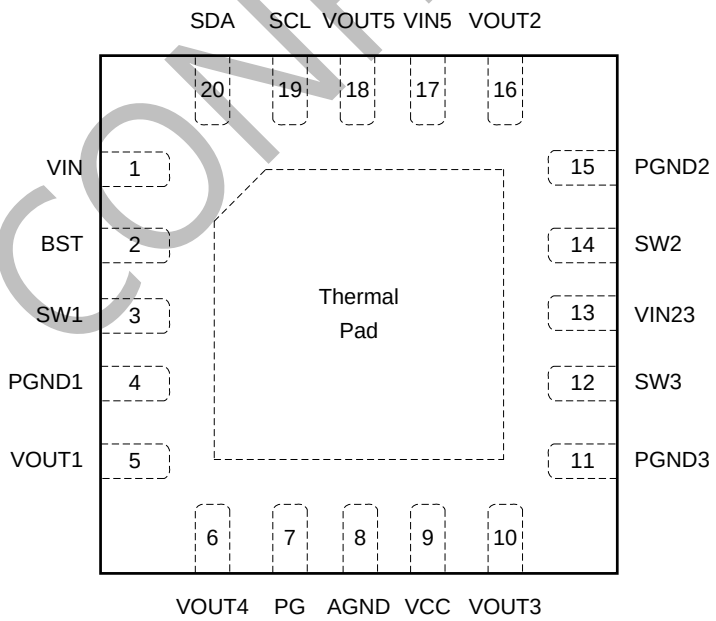
1) "xxxx" is the specific suffix code for different configuration. Contact SCT for details.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	21	V
SW1	-0.3(-1 in 30ns)	21	V
BST-SW1	-0.3	6	V
Others	-0.3	6	V
Operating junction temperature T_J (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View : 20-Lead QFN 3mm×3mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes thermal shutdown protection to protect the device during overload conditions. Junction temperature will exceed 170°C when thermal shutdown protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	PIN	PIN FUNCTION
VIN	1	Input supply for the device and Buck1. A decoupling capacitor to ground is recommended to be placed close to VIN pin to minimize switching spikes.
BST	2	Bootstrap capacitor connection pin for Buck1. Connect a 0.1uF ceramic capacitor between this pin and SW1.
SW1	3	Buck1 switch node. SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
PGND1	4	Power ground for Buck1. Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
VOUT1	5	Feedback for Buck1 and power source for LDO4. Connect VOUT1 pin to Buck1 output directly. A decoupling capacitor to ground is recommended to be placed close to VOUT1 pin to minimize switching spikes.
VOUT4	6	LDO4 output. Connect a 4.7uF ceramic capacitor or higher between this pin and ground.
PG	7	Open-drain power good indication. High state of this pin indicates all channels work properly and low state indicates power rails are not ready or a fault condition. Connect this pin to high level through a pull-up resistor. Float this pin if not used.
AGND	8	Analog ground. AGND is the reference GND for the internal logic and signal circuit. AGND is not internally connected to power ground. Make sure AGND connected to power ground in PCB.
VCC	9	Internal VCC regulator output. Power supply to the internal control circuit and gate drivers. A 1uF capacitor to ground close to this pin is required.
VOUT3	10	Feedback for Buck 3. Connect VOUT3 pin to the Buck3 output directly.
PGND3	11	Power ground for Buck 3. Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
SW3	12	Buck 3 switch node. SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
VIN23	13	Input supply for Buck2 and Buck3. VIN23 is assumed to be connected to the output of Buck1. Place a 10 F ceramic decoupling capacitor or higher close to VIN23 pin.
SW2	14	Buck 2 switch node. SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
PGND2	15	Power ground for Buck 2. Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
VOUT2	16	Feedback for Buck 2. Connect VOUT2 pin to the Buck2 output directly.
VIN5	17	Input supply for LDO5. Place a 4.7 F ceramic decoupling capacitor or higher close to VIN5 pin.
VOUT5	18	LDO5 output. Connect a 4.7uF ceramic capacitor between this pin and ground.
SCL	19	Serial clock line. Connect this pin to ground if not used.
SDA	20	Serial data line. Open-Drain I/O. Connect this pin to high level with a pull-up resistor. Connect this pin to ground if not used.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted.

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	VIN Input voltage range	4	19	V
V_{IN23}	VIN23 Input voltage range	3	4	V
V_{IN5}	VIN5 Input voltage range	1	4	V
V_{OUT1}	HV Buck1 output voltage range	3.1	4	V
V_{OUT2}	LV Buck2 output voltage range	1.1	3.3	V
V_{OUT3}	LV Buck3 output voltage range	0.6	1.8	V
V_{OUT4}	LDO4 output voltage range	2.7	3.3	V
V_{OUT5}	LDO5 output voltage range	0.8	3.3	V
T_J	Operating junction temperature	-40	150	°C

ESDRATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC-Q100-002	-2	+2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	+1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-20L	UNIT
R_{JA}	Junction to ambient thermal resistance(1)	55.52	°C/W
$_{JT}$	Junction-to-top characterization parameter(1)	5.7	
$_{JB}$	Junction-to-board characterization parameter(1)	12.06	
$R_{JC(top)}$	[redacted]		

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{LIM_LSP2}	Low-side switch valley current limit			1.8		A
I_{LIM_LSN2}	Low-side reverse current limit			1.3		A
R_{DIS2}	Output discharge resistance	Output disabled		70		
t_{ON_MIN2}(1)	Minimum on-time			60		ns
LV BUCK3						
V_{IN23}	Supply voltage range		3		4	V
V_{OUT3}	Output voltage configurable range		0.6		1.8	V
V_{OUT3_ACC}	Output voltage accuracy		-2		+2	%
R_{DSON_HS3}	High-side switch on-resistance			220		m
R_{DSON_LS3}	Low-side switch on-resistance			120		m
I_{LIM_HS3}	High-side switch peak current limit			2		A
I_{LIM_LSP3}	Low-side switch valley current limit			1.8		A
I_{LIM_LSN3}	Low-side reverse current limit			1.3		A
R_{DIS3}	Output discharge resistance	Output disabled		70		
t_{ON_MIN3}(1)	Minimum on-time			60		ns
LDO4						
V_{LDO4}	Output voltage configurable range		2.7		3.3	V
V_{LDO4_ACC}	Output voltage accuracy		-2		+2	%
V_{LDO4_DROP}	Dropout voltage	V_{OUT1}=3.3V, V_{LDO4} set to 3.3V, I_{LDO4}=300mA		110		mV
L_{LINE_REG4}	Line Regulation	V_{OUT1}=3.1V to 4V, V_{LDO4} set to 2.8V, I_{LDO4}=100mA		0.01		%/V
L_{LOAD_REG4}	Load Regulation	V_{OUT1}=3.3V, V_{LDO4} set to 2.8V, I_{LDO4}=10mA to 300mA		0.2		%
I_{LIM_OCP4}	Over current limit	V_{OUT1}=3.3V, V_{LDO4} set to 2.8V		400		mA
PSRR(1)	Power supply rejection ratio	V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=50mA, @ 1kHz		60		dB
		V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=50mA, @ 10kHz		60		dB
		V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=50mA, @ 100kHz		60		dB
		V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=50mA, @ 1MHz		40		dB
N_{RMS}(1)	RMS noise	V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, from 10Hz to 100kHz		30		V_{RMS}
R_{DIS4}	Output discharge resistance	Output disabled		70		

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
LDO5						
V_{IN5}	Supply voltage range		1		4	V
V_{LDO5}	Output voltage configurable range		0.8		3.3	V
V_{LDO5_ACC}	Output voltage accuracy		-2		+2	%
V_{LDO5_DROP}	Dropout voltage	V_{IN5}=1.8V, V_{LDO5} set to 1.8V, I_{LDO5}=300mA		140		mV
L_{LINE_REG5}	Line Regulation	V_{IN5}=1.3V to 4V, V_{LDO5} set to 1V, I_{LDO5}=100mA		0.01		%/V
L_{LOAD_REG5}	Load Regulation	V_{IN5}=1.8V, V_{LDO5} set to 1V, I_{LDO5}=10mA to 300mA		0.8		%
I_{LIM_OCP5}	Over current limit	V_{IN5}=1.8V, V_{LDO5} set to 1V		400		mA
R_{DIS5}	Output discharge resistance			70		
Protection						
V_{OUT1_OVP}	Buck1 output over-voltage rising threshold	OV1[1:0]=00		105		%
		OV1[1:0]=01		110		%
		OV1[1:0]=10		115		%
		OV1[1:0]=11		120		%
V_{OUT1_UVP}	Buck1 output under-voltage falling threshold	UV1[1:0]=00		95		%
		UV1[1:0]=01		90		%
		UV1[1:0]=10		85		%
		UV1[1:0]=11		80		%
$V_{OUT2/3/4/5\_OVP}$	Buck2/3/LDO4/5 output over-voltage rising threshold	OV2/3/4/5[1:0]=01		105		%
		OV2/3/4/5[1:0]=10		106		% 494 38..94 0.48.48

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency				1	MHz
t_{LOW}	Low period of the SCL clock		500			ns
t_{HIGH}	High period of the SCL clock		260			ns
t_{HD_STA}	Hold time (repeated) START condition		260			ns
t_{SU_STA}	Set-up time for a repeated START condition		260			ns
t_{HD_DAT}	Data hold time		0			ns
t_{SU_DAT}	Data set-up time		50			ns
t_{SU_STO}	Set-up time for STOP condition		260			ns
t_r	Rise time of both SCL and SDA signals				120	ns
t_f	Fall time of both SCL and SDA signals				120	ns
C_B	Capacitive load for each bus line				550	pF

(1) Guaranteed by sample characterization, not tested in production.

TYPICALCHARACTERISTICS

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, V_{OUT5} = 1V, L1 = 2.2uH, L2 = L3 = 1uH, T_A = 25°C, unless otherwise noted.

Figure 1. Buck1 Efficiency vs. Load Current

Figure 2. Buck1 Load Regulation

Figure 3. Buck2 Efficiency vs. Load Current

Figure 4. Buck2 Load Regulation

Figure 5.

TYPICAL CHARACTERISTICS (continued)

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, V_{OUT5} = 1V, L1 = 2.2uH, L2 = L3 = 1uH, T_A = 25°C, unless otherwise noted.

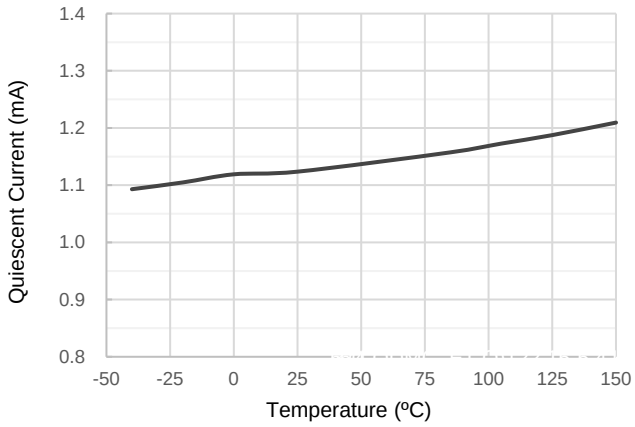


Figure 7. Quiescent Current (rails off) vs. Temperature

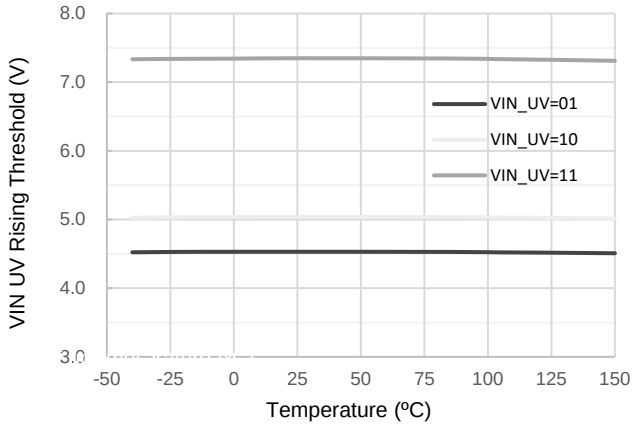


Figure 8. VIN UV Rising Threshold vs. Temperature

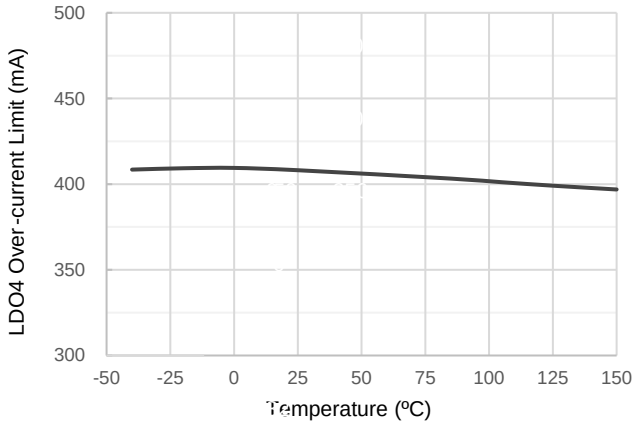


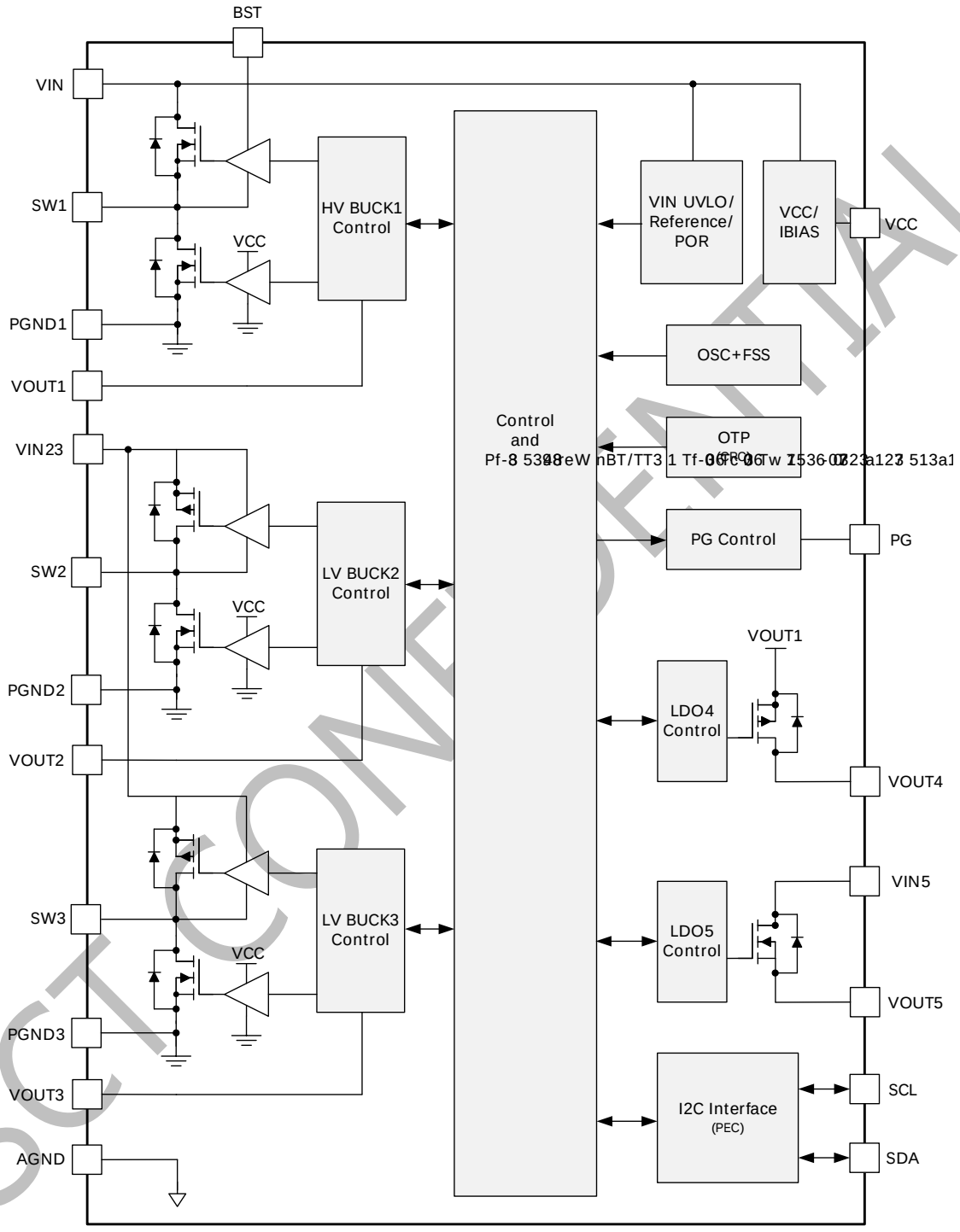
Figure 9. LDO4 Over-current Limit vs. Temperature

Figure 10. LDO4 Dropout Voltage vs. Temperature

Figure 11. LDO5 Over-current Limit vs. Temperature

Figure 12. LDO5 Dropout Voltage vs. Temperature

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Overview

The SCT61250S is a highly integrated power management IC (PMIC) optimized for automotive camera system. It integrates three high-efficiency synchronous buck converters (HV Buck1, LV Buck2, LV Buck3), one high-PSRR low noise LDO (LDO4) and one general LDO (LDO5) with over-voltage/under-voltage monitoring on all outputs. The output voltage and power sequence of each channel are pre-programmed to achieve a flexible and minimized power

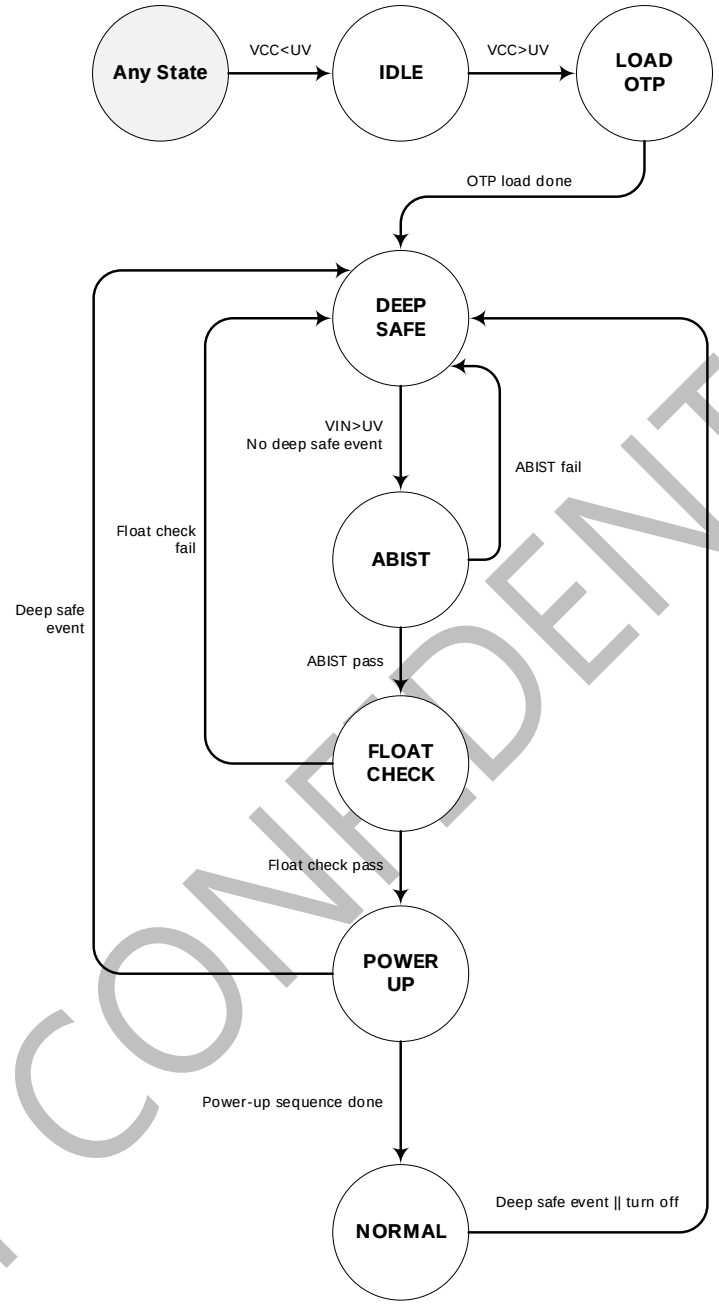


Figure 14. Operating State Machine and Transitions

DEEPSAFE State

In DEEPSAFE state, all channels are off and PG pin is low. The device is held and waits for all conditions met to power up. To exit DEEPSAFE state, VIN should be higher than V_{IN_UV} threshold, OTP CRC shall pass and no other critical fault like thermal shutdown is triggered. For a normal power-on, the device will transit to ABIST state almost immediately if all conditions are met when entering DEEPSAFE state. The device would also enter DEEPSAFE state when any of the deep safe events shown in Table 2 occurs after startup. After a deep safe event triggered, all power rails are shut down immediately and simultaneously while I2C interface keeps alive, allowing user to

communicate with the device and read the status registers to locate the specific fault. The device will stay in DEEPSAFE state in latch mode, or transit to ABIST state once the deep safe event discontinued and the hiccup timer expired in hiccup mode. The latch or hiccup mode could be selected in PROT_MODE[0].

Table 2. Deep Safe Event

Category	Deep Safe Event	Status Bit
Analog	Buck1 output is out of OV/UV range.	OV1[0], UV1[0]
	Buck2 output is out of OV/UV range.	OV2[0], UV2[0]
	Buck3 output is out of OV/UV range.	OV3[0], UV3[0]
	LDO4 output is out of OV/UV range.	OV4[0], UV4[0]
	LDO5 output is out of OV/UV range.	OV5[0], UV5[0]
	VIN is below under-voltage threshold.	VIN_UV[0]
	VIN is above over-voltage threshold.	VIN_OV[0]
	VIN23 is above over-voltage threshold (typ. 5.4V).	VIN23_OV[0]
	VIN5 is above over-voltage threshold (typ. 5.4V).	VIN5_OV[0]
	VCC is above over-voltage threshold.	VCC_OV[0]
	VOUT1/2/3 pin float error.	VOUT1_FLT[0], VOUT2_FLT[0], VOUT3_FLT[0]
	ABIST error.	ABIST_ERR[0]
	Thermal shutdown.	TSD[0]
Digital	OTP CRC error.	OTP_CRC_ERR[0]
	Online CRC error.	ONLINE_CRC_ERR[0]
	Internal clock error.	CLK_MON_ERR[0]

ABIST State

To ensure safety mechanism works well, the device will check through all critical analog comparators before power rails built up. ABIST (Analog Built-in Self Test) will be implemented every time the device enters ABIST state. If ABIST check fails, the device will transit back to DEEPSAFE state, and if ABIST passes, the device will transit to FLOATCHECK state. Any error found during ABIST will be recorded in register bit ABIST_ERR[0].

FLOATCHECK State

The device will check if VOUT1, VOUT2 and VOUT3 pins are floating before power rails built up. The device will transit to POWERUP state to continue startup if no pin float error found, or jump to DEEPSAFE state if any pin float error found.

POWERUP State

In POWERUP state, all power rails will be built up following the OTP-programmed sequence. HV Buck1 is always the first one to power up, and the other channels then will start up one-by-one according to the configuration in SEQ[4:0]. The soft-start time of each channel could be selected in SS_TIME[0]. If all channels finish soft-start within power good range, the PG rising delay timer starts and the duration is configured in PG_DLY[0]. Once the timer is expired, the device will enter NORMAL state and PG pin will be pulled high. See Figure 18 for a detailed power-on sequence. If any deep safe event occurs in POWERUP state, the device will transit to DEEPSAFE state directly.

NORMAL State

Normal state is the normal operation state of the device with all enabled channels on. PG pin is pulled high upon

entering the state and all output rails are continuously monitored. When operating in NORMAL state, the device will transit to DEEPSAFE state once any deep safe event occurs.

High Efficiency Buck Converters

All three buck converters employ 2.1MHz fixed frequency peak current mode control. The forced continuous conduction mode realizes low output voltage ripple and good transient response at all load condition. The output voltage, power sequence, soft-start time and loop compensation are pre-programmed without any setting by external components, which makes the device easy to use by minimizing the off-chip component count.

For Buck1, an external 100nF bootstrap capacitor between BST and SW1 pin is required to power high-side power switch gate driver. The bootstrap capacitor is charged from an integrated regulator when high-side power switch is off and low-side power switch is on.

The buck converters have proprietary designed gate driver scheme to resist switching node ringing without sacrificing switch turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the switch hard switching.

Under-voltage /Over-voltage Protection

If any channel's output falls below the under-voltage protection threshold or exceeds the over-voltage protection threshold, all channels will shut off, and then keep off in latch mode or automatically restart in hiccup mode, which is set by PROT_MODE[0]. For latch mode, the device will only restart after a power recycle. For hiccup mode, the

Frequency Spread Spectrum

To meet CISPR and automotive EMI compliances, the SCT61250S implements Frequency Spread Spectrum (FSS) function. The FSS circuitry shifts the 2.1MHz switching frequency of three buck converters within ±5/±10% range and 4.5/9kHz period, which are configured in FSS_RANGE[0] and FSS_PERIOD[0]. The FSS feature guarantees the switching frequency does not drop into 1.8MHz AM band limit.

Active O

I2C Interface

The SCT61250S integrates a two-wire serial interface for bidirectional communications between the device and the master through the bus. The I2C protocol defines two bus lines, the serial data line (SDA) and the serial clock line (SCL). The device is assigned with a unique chip address 0x38 by default and operates as a slave. The master drives the SCL line and transfer bidirectional data through SDA line. Both the SCL and the SDA lines need a pull-up resistor connected to bus voltage since high state is the default state

Packet Error Checking (PEC)

The SCT61250S supports optional packet error checking (PEC) byte during the I2C communication. PEC can significantly increase fault coverage on the I2C interface. The PEC byte is implemented through CRC-8 polynomial of x8 + x2 + x +1. The PEC byte does not take ACK, NACK, START, STOP, Repeated START bits into calculation. The PEC byte is calculated with the register address and data byte over the entire message from the first START condition. Note that the slave address is not involved in the calculation both in write and read command. When PEC is enabled, the device will reject the write command if the master send an incorrect PEC byte. When in read mode with PEC enabled, the master should acknowledge the data byte thus then the device will send the PEC byte. PEC function can be enabled or disabled by PEC_EN[0].

Write Data Format

A write to the device includes transmission of the following:

- START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- 1 byte of data to the command register
- STOP condition

Read Data Format

A read from the device includes the following:

- Transmission of a START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- Restart condition
- Slave address with read bit set to 1
- 1 byte of data to the command register
- STOP condition

Figure 17 illustrates the proper format for one frame.

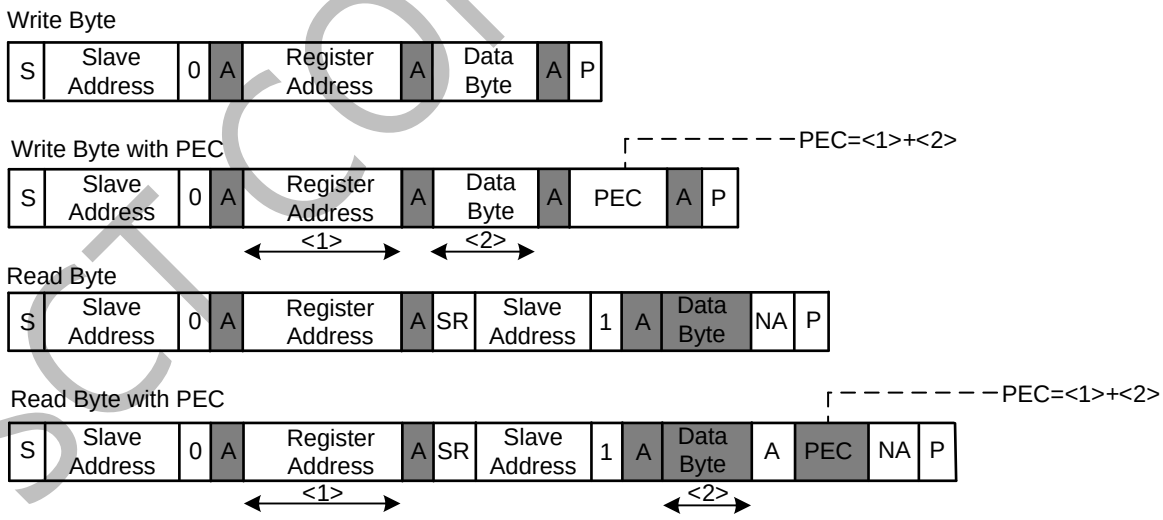


Figure 17. Transmission Data Format

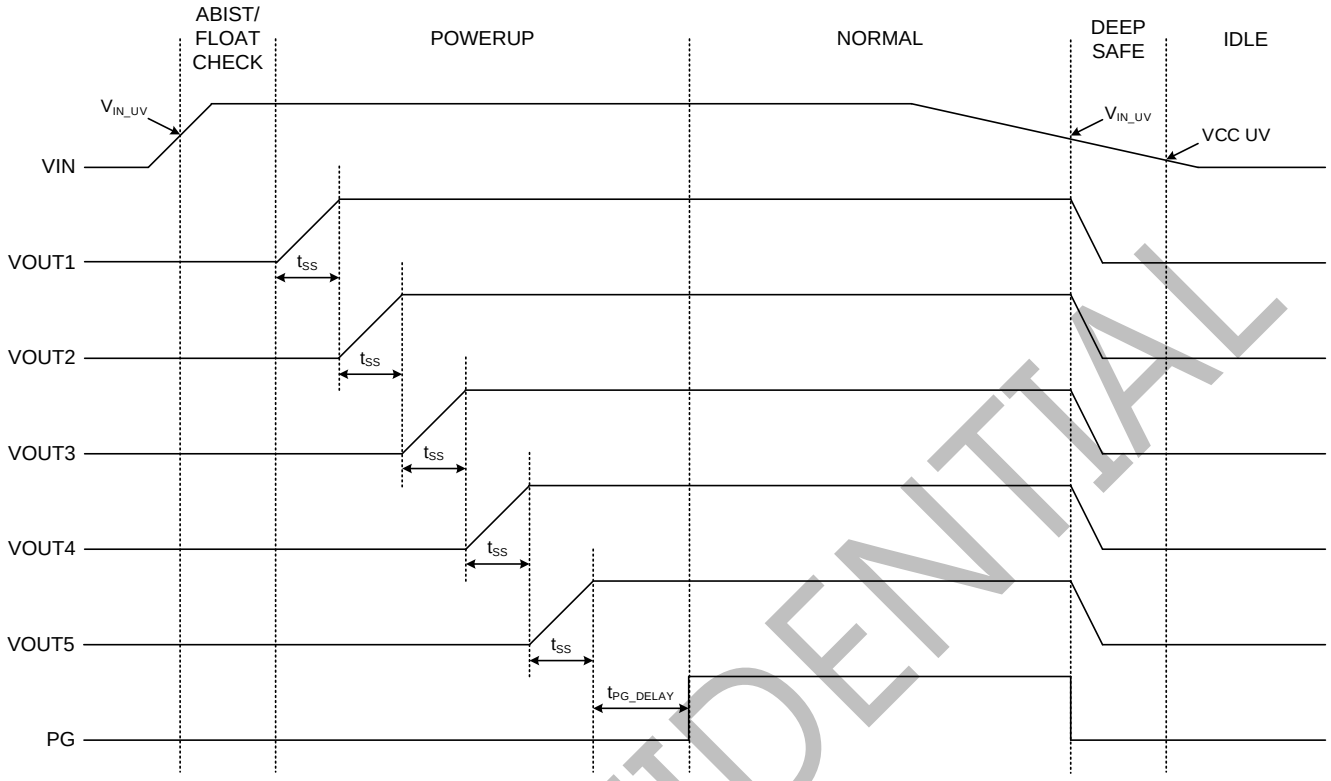


Figure 18. Power On/Off Sequence

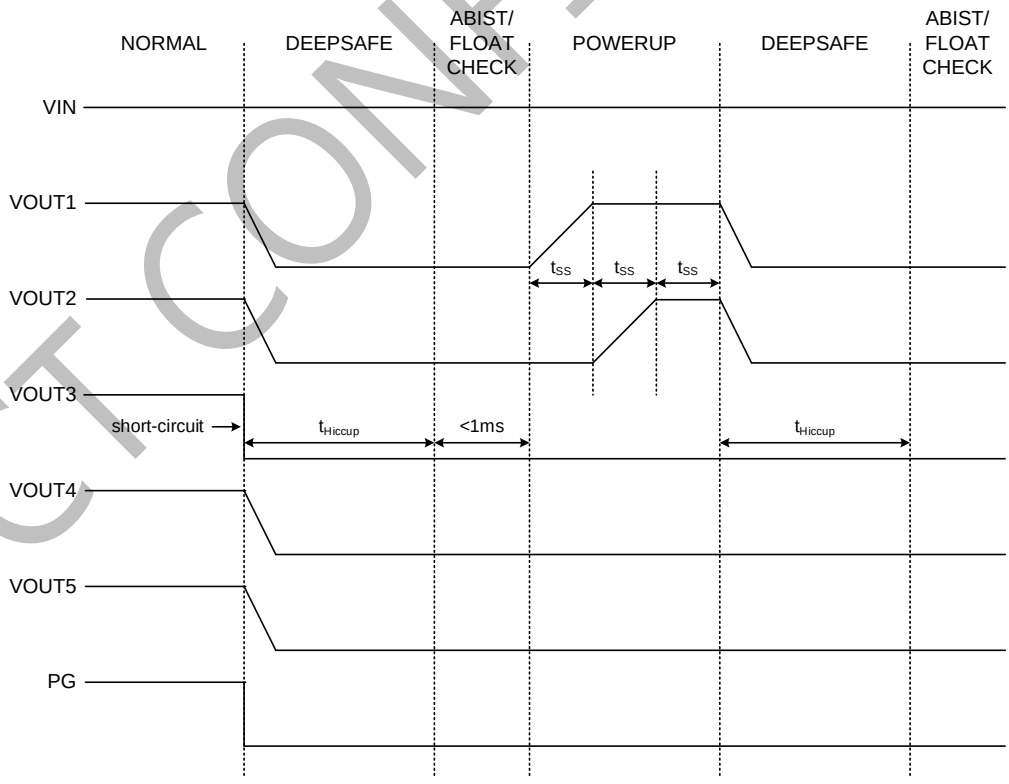


Figure 19. Deep Safe Event in Hiccup Mode

Table 3. Recommended BOM for Typical Application

Power Rail	Switching Frequency	Inductor	Output Capacitor
Buck1	2.1MHz	2.2uH	10uF
Buck2	2.1MHz	1uH	10uF
Buck3	2.1MHz	1uH	10uF (V_{OUT3} > 1V) 20uF (V_{OUT3} 1V)
LDO4	-	-	4.7uF
LDO5	-	-	4.7uF

Application Waveforms

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, V_{OUT5} = 1V, L1 = 2.2uH, L2 = L3 = 1uH, T_A = 25°C, unless otherwise noted.

Figure 21. Power On Sequence I

Figure 22. Power Off Sequence I

Figure 23. Power On Sequence II

Figure 24. Power Off Sequence II

Figure 25. Buck1 Steady State, Load=1.2A

Figure 26. Buck2 Steady State, Load=1.2A

Application Waveforms (continued)

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, V_{OUT5} = 1V, L1 = 2.2uH, L2 = L3 = 1uH, T_A = 25°C, unless otherwise noted.

Figure 27. Buck3 Steady State, Load=1.2A

Figure 28. Buck1 Short-circuit and Recovery

Figure 29. Buck2 Short-circuit and Recovery

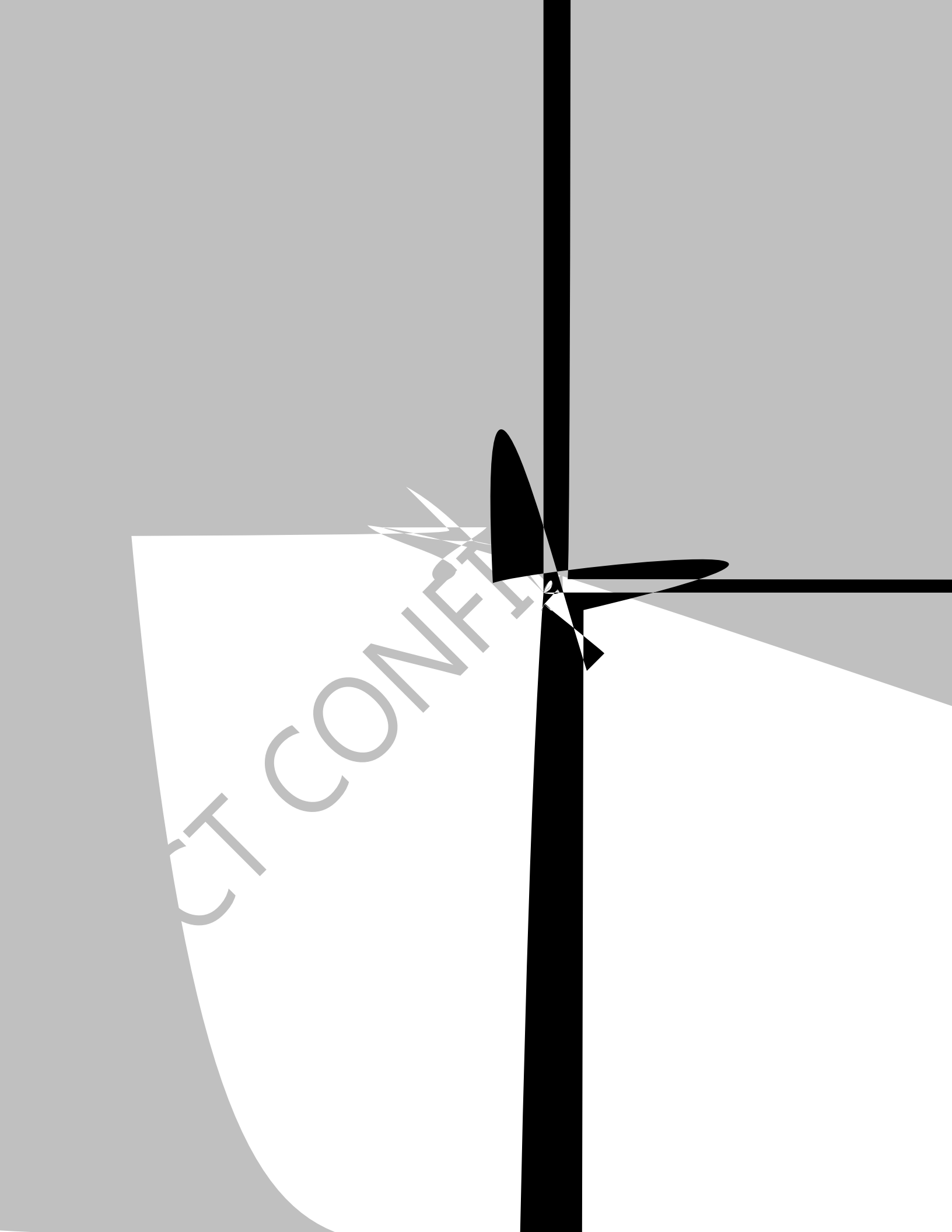
Figure 30. Buck3 Short-circuit and Recovery

Figure 31. LDO4 Short-circuit and Recovery

Figure 32. LDO5 Short-circuit and Recovery

Layout Guideline

Proper PCB layout is critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:


CT CONFI

REGISTER DESCRIPTION

CHIPID [7:0]			
ADDRESS: 0x00			
BITS	FIELD	TYPE	DESCRIPTION
[7:0]	CONFIG_ID	R	Chip Configuration Identification. This is a unique number identifying the factory configuration of the device. This helps identify/verify the configuration without having to look at all configuration registers.

CTRL_EN [7:0]			
ADDRESS: 0x01			
BITS	FIELD	TYPE	DESCRIPTION
[7]	PEC_EN	W/R	Packet Error Checking Enable. Set this bit to 1 to enable PEC or 0 to disable PEC. 0: Disabled 1: Enabled
[6]	HIC_TIME	W/R	Hiccup time selection for hiccup mode. After any protection triggered, the device will keep all channels off for at least this hiccup time and then start a new power-up sequence. 0: 3ms 1: 10ms
[5]	PROT_MODE	W/R	Protection mode selection. 0: Hiccup Mode 1: Latch Mode
[4]	EN5	W/R	Enable for LDO5. 0: Disabled 1: Enabled
[3]	EN4	W/R	Enable for LDO4. 0: Disabled 1: Enabled
[2]	EN3	W/R	Enable for LV Buck3. 0: Disabled 1: Enabled
[1]	EN2	W/R	Enable for LV Buck2. 0: Disabled 1: Enabled
[0]	EN_ALL	W/R	Enable for all channels. 0: Disabled 1: Enabled

CONFIG_SYS1 [7:0]			
ADDRESS: 0x02			
BITS	FIELD	TYPE	DESCRIPTION
[7]	FSS_PERIOD	W/R	Frequency spread spectrum period. 0: 4.5kHz 1: 9kHz
[6]	FSS_RANGE	W/R	Frequency spread spectrum range. 0: ±5% 1: ±10%
[5]	FSS_EN	W/R	Enable for frequency spread spectrum. 0: Disabled 1: Enabled
[4]	RESERVED	R	/
[3:2]	OVUV_DEG	W/R	OV rising/UV falling deglitch time for all output monitors. 00: 40us 01: 80us 10: 120us 11: 160us
[1:0]	VIN_UV	W/R	VIN under-voltage lockout threshold selection. 00: Reserved 01: Rising=4.5V / Falling=4V 10: Rising=5.0V / Falling=4.5V 11: Rising=7.3V / Falling=6.8V

CONFIG_SYS2 [7:0]			
ADDRESS: 0x03			
BITS	FIELD	TYPE	DESCRIPTION
[7:6]	OV5	W/R	LDO5 output over-voltage threshold selection. 00: Reserved 01: 105% 10: 106% 11: 110%
[5:4]	OV4	W/R	LDO4 output over-voltage threshold selection. 00: Reserved 01: 105% 10: 106% 11: 110%
[3:2]	OV3	W/R	Buck3 output over-voltage threshold selection. 00: Reserved 01: 105% 10: 106% 11: 110%
[1:0]	OV2	W/R	Buck2 output over-voltage threshold selection. 00: Reserved 01: 105% 10: 106% 11: 110%

CONFIG_SYS3 [7:0]			
ADDRESS: 0x04			
BITS	FIELD	TYPE	DESCRIPTION
[7:6]	OV1	W/R	Buck1 output over-voltage threshold selection. 00: 105% 01: 110% 10: 115% 11: 120%
[5:4]	UV5	W/R	LDO5 output under-voltage threshold selection. 00: Reserved 01: 95% 10: 94% 11: 90%
[3:2]	UV4	W/R	LDO4 output under-voltage threshold selection. 00: Reserved 01: 95% 10: 94% 11: 90%
[1:0]	UV3	W/R	Buck3 output under-voltage threshold selection. 00: Reserved 01: 95% 10: 94% 11: 90%

CONFIG_SYS4 [7:0]			
ADDRESS: 0x05			
BITS	FIELD	TYPE	DESCRIPTION
[7:6]	UV2	W/R	Buck2 output under-voltage threshold selection. 00: Reserved 01: 95% 10: 94% 11: 90%
[5:4]	UV1	W/R	Buck1 output under-voltage threshold selection. 00: 95% 01: 90% 10: 85% 11: 80%
[3:0]	RESERVED	R	/

CONFIG_VO145 [7:0]			
ADDRESS: 0x06			
BITS	FIELD	TYPE	DESCRIPTION
[7:5]	VOUT1	R	Buck1 output voltage setting. 000: 3.1V

STATUS1 [7:0]			
ADDRESS: 0x09			
BITS	FIELD	TYPE	DESCRIPTION
[7]	UV5	W1C/R	LDO5 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[6]	UV4	W1C/R	LDO4 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[5]	UV3	W1C/R	Buck3 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[4]	UV2	W1C/R	Buck2 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[3]	UV1	W1C/R	Buck1 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[2]	OV5	W1C/R	LDO5 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[1]	OV4	W1C/R	LDO4 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	OV3	W1C/R	Buck3 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.

STATUS2 [7:0]			
ADDRESS: 0x0A			
BITS	FIELD	TYPE	DESCRIPTION
[7]	OV2	W1C/R	Buck2 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[6]	OV1	W1C/R	Buck1 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[5:1]	RESERVED	R	/
[0]	VOUT1_FLT	W1C/R	VOUT1 pin float status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.

STATUS3 [7:0]			
ADDRESS: 0x0B			
BITS	FIELD	TYPE	DESCRIPTION
[7]	VOUT2_FLT	W1C/R	VOUT2 pin float status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[6]	VOUT3_FLT	W1C/R	VOUT3 pin float status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[5]	VIN_OV	W1C/R	VIN over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[4]	VIN23_OV	W1C/R	VIN23 over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[3]	VIN5_OV	W1C/R	VIN5 over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[2]	VCC_OV	W1C/R	VCC over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[1]	TSD	W1C/R	Thermal shutdown status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	I2C_PEC_ERR	W1C/R	I2C PEC error status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.

STATUS4 [7:0]			
ADDRESS: 0x0C			
BITS	FIELD	TYPE	DESCRIPTION
[7:6]	RESERVED	R	/
[5]	ABIST_ERR	W1C/R	ABIST fault status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[4]	ONLINE_CRC_ERR	W1C/R	Online register CRC fault status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[3]	OTP_CRC_ERR	W1C/R	OTP CRC fault status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[2]	CLK_MON_ERR	W1C/R	Internal clock fault status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[1]	VIN_UV	W1C/R	VIN under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	RESERVED	R	/

STATE [7:0]			
ADDRESS: 0x1F			
BITS	FIELD	TYPE	DESCRIPTION
[7:3]	RESERVED	R	/
[2:0]	SYS_STATE	R	System state machine real-time status. 000: IDLE 001: LOADOTP 010: ABIST 011: Reserved 100: DEEPSAFE 101: NORMAL 110: FLOATCHECK 111: POWERUP

I2C_LOCK [7:0]			
ADDRESS: 0x3F			
BITS	FIELD	TYPE	DESCRIPTION
[7:1]	RESERVED	R	/
[0]	I2C_LOCK	W/R	Write “1” to this bit to unlock I2C write operation for registers under protection (see Register Map), or “0” to lock it off. When I2C write operation is locked, online CRC is automatically activated to verify all the register data.

PACKAGE INFORMATION

TAPE AND REEL INFORMATION

